FIG. 1a

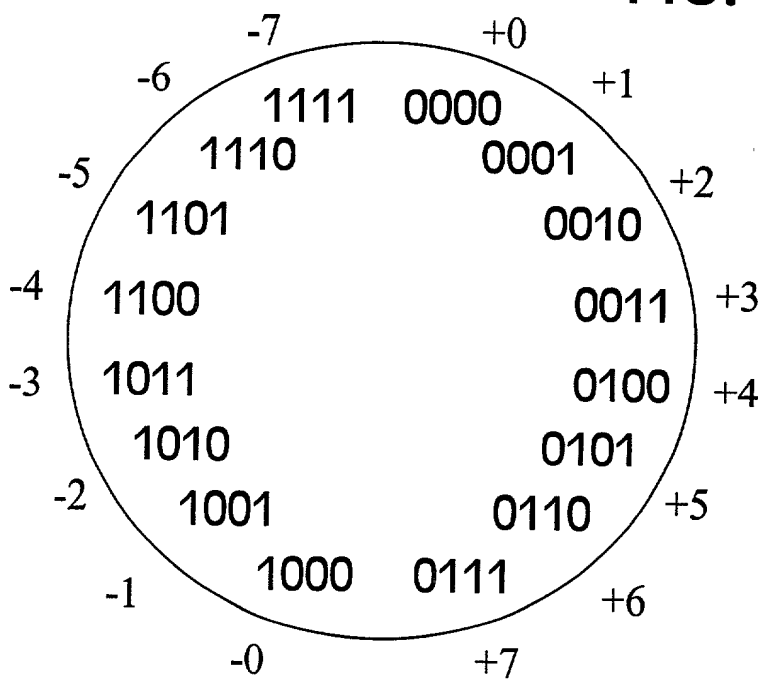
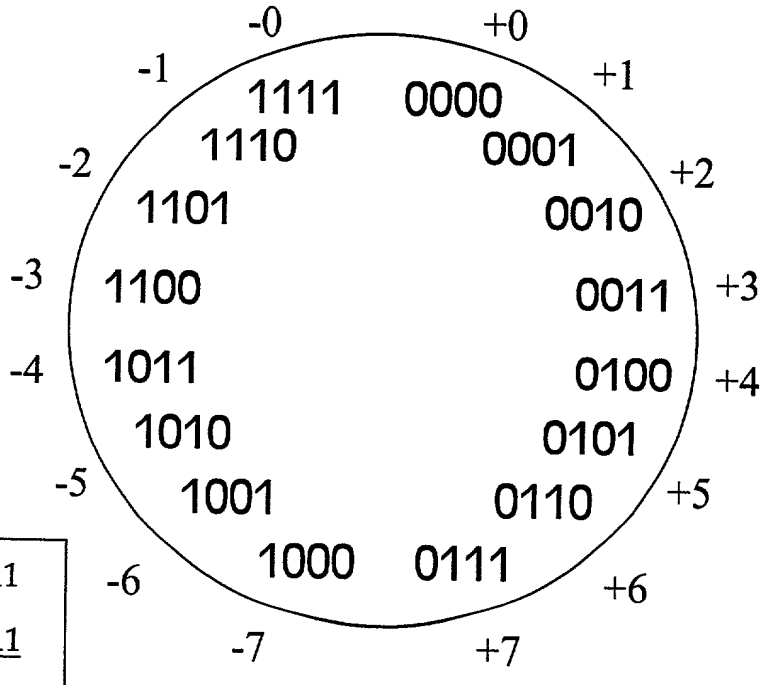


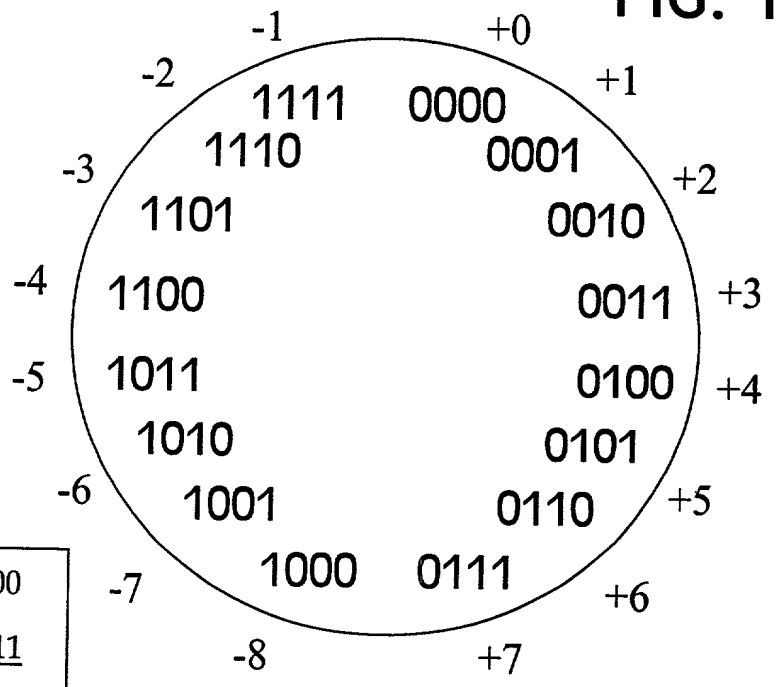
FIG. 1b



$2^4 - 1 =$	15	1111
subtract	7	- 0111
to get	-7	1000

120

FIG. 1c



2^4 =	16	10000
subtract	7	- 0111
to get	-7	1001

130

FIG. 2

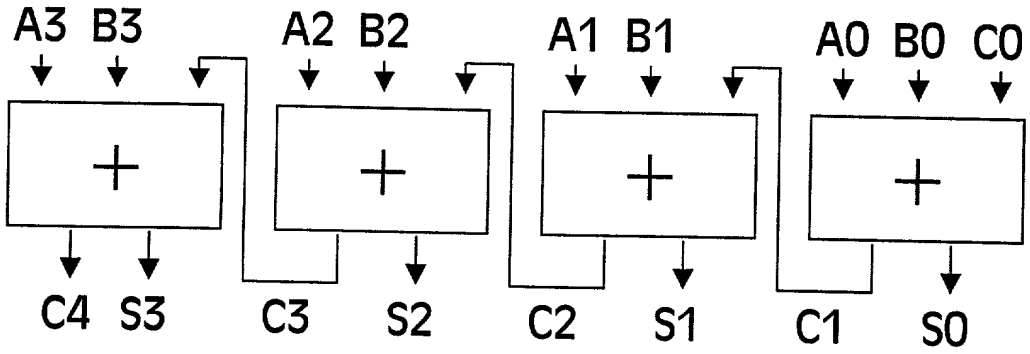


FIG. 3a

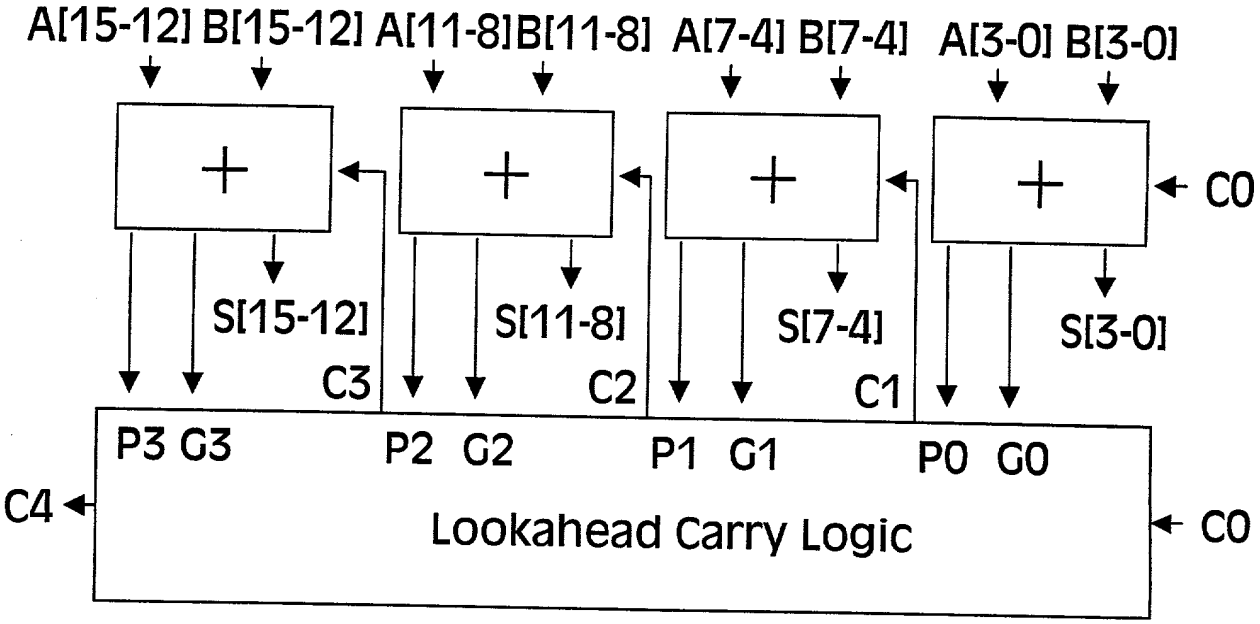

A[15-12]
B[15-12]
A[11-8]
B[11-8]
A[7-4]
B[7-4]
A[3-0]
B[3-0]
C0
S[15-12]
S[11-8]
S[7-4]
S[3-0]
C3
C2
C1
P3 G3
P2 G2
P1 G1
P0 G0
C4
Lookahead Carry Logic
C0

FIG. 3b

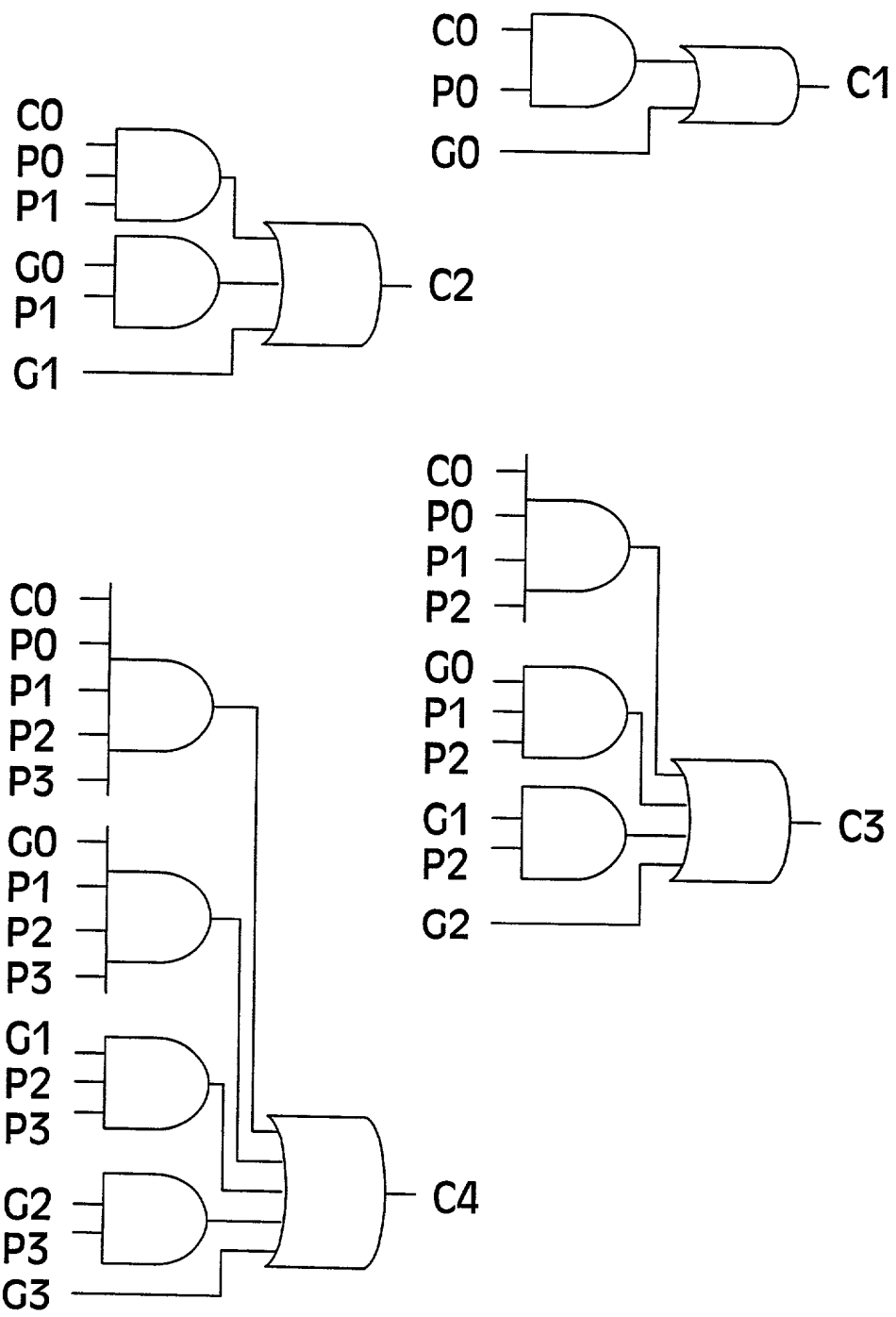
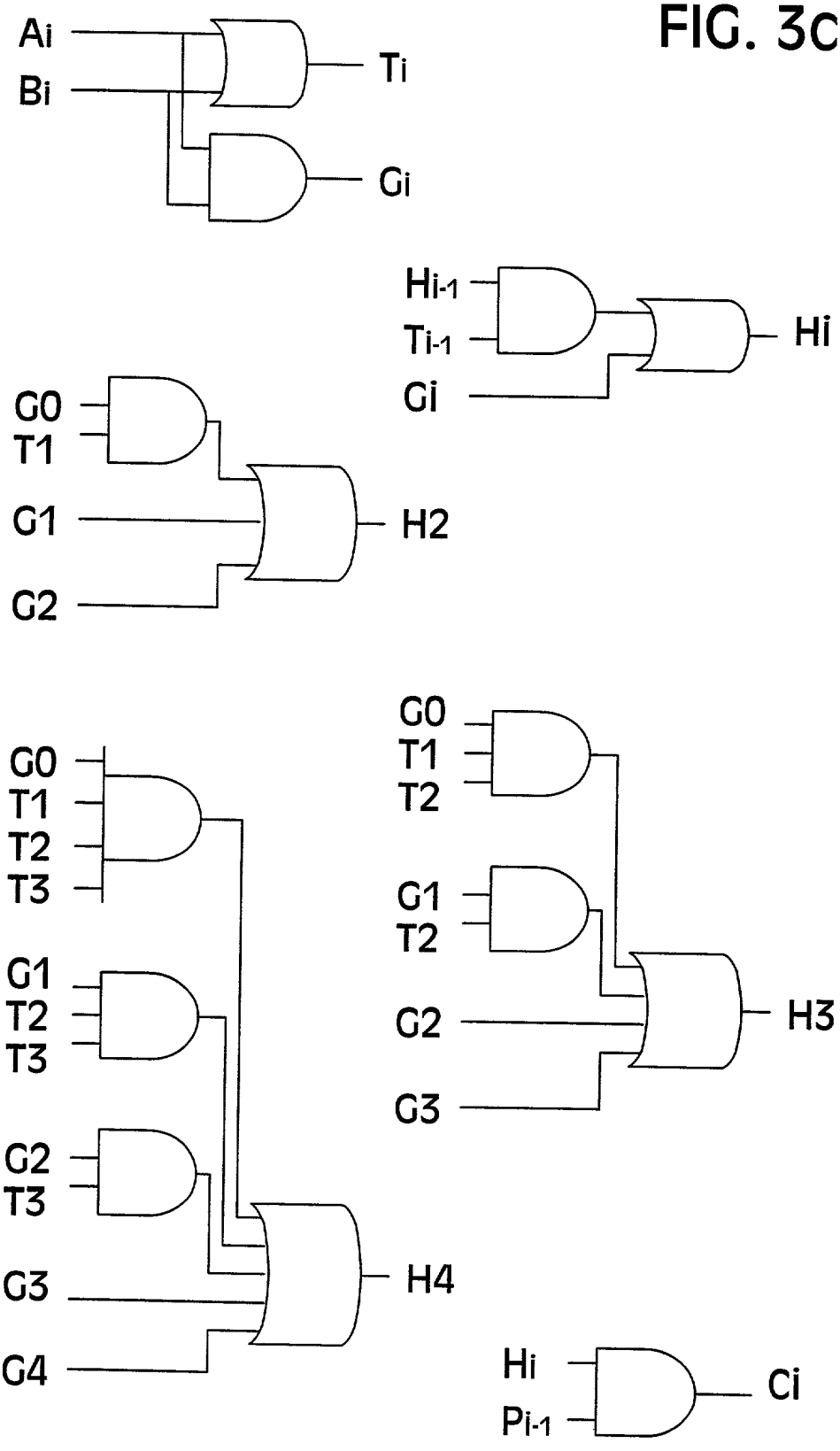
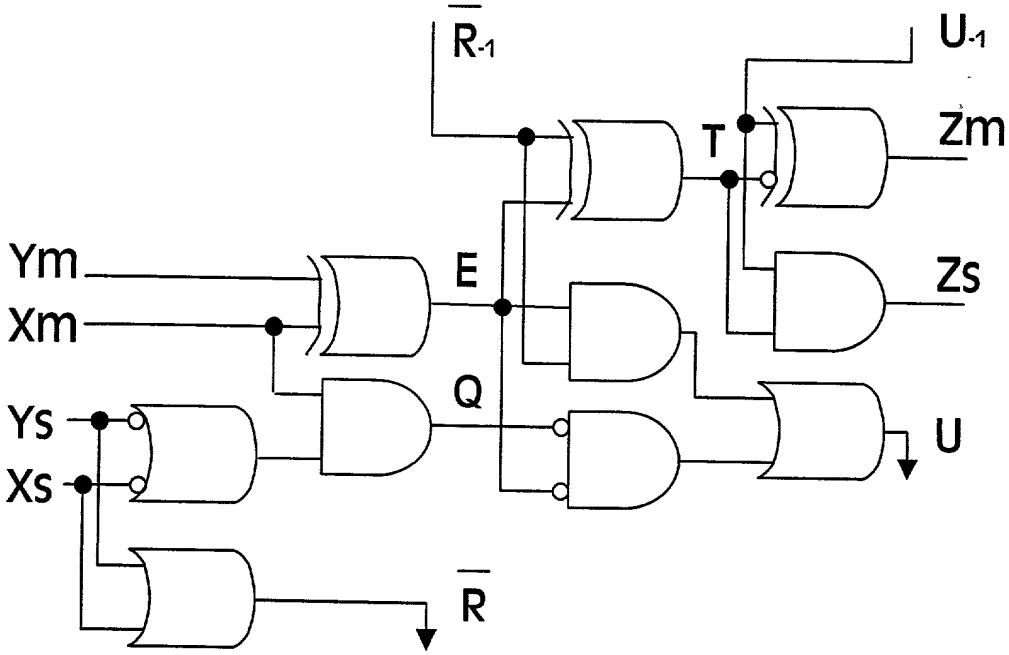

C0
P0
G0
C1
C0
P0
P1
G0
P1
G1
C2
C0
P0
P1
P2
G0
P1
P2
G1
P2
G2
C3
C0
P0
P1
P2
P3
G0
P1
P2
P3
G1
P2
P3
G2
P3
G3
C4

FIG. 3C


Ai
Bi
Ti
Gi
Hi-1
Ti-1
Gi
Hi
G0
T1
G1
G2
H2
G0
T1
T2
T3
G1
T2
T3
G2
T3
G3
G4
H4
G0
T1
T2
G1
T2
G2
G3
H3
Hi
Pi-1
Ci

PRIOR ART

FIG. 4



PRIOR ART

FIG. 5

Pair i	0 +0	1 +1	-1 +-1	
Pair i -1	any	any	any	
Output	$C_i=0$ $U_i=0$	$C_i=1$ $U_i=0$	$C_i=-1$ $U_i=0$	

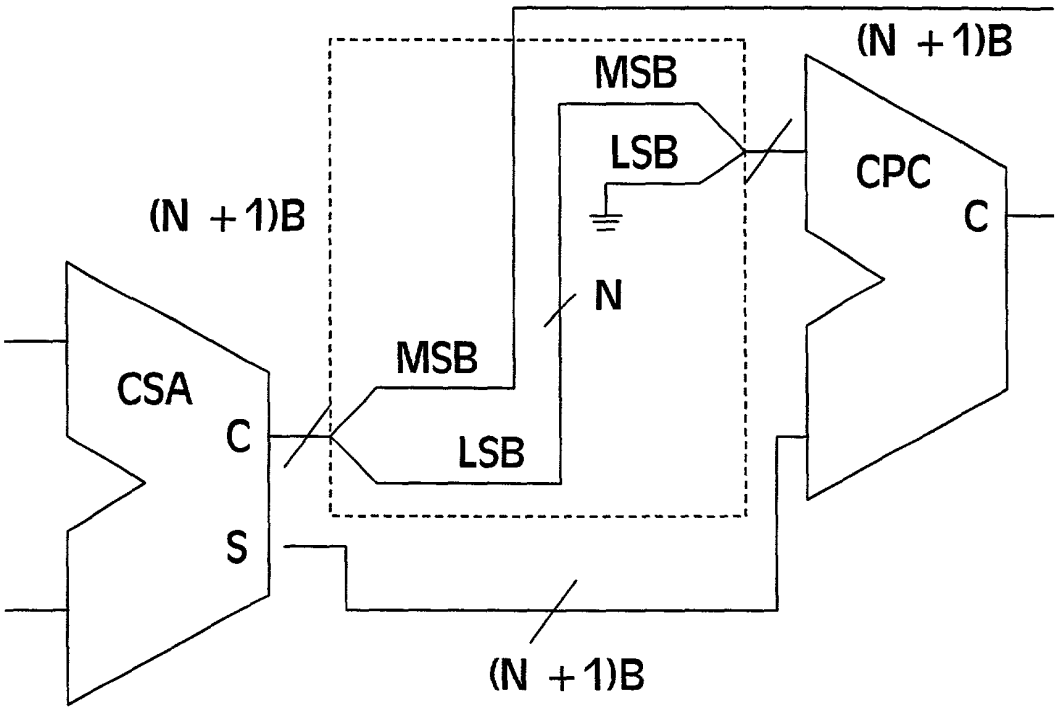
Pair i	0 +1	-1 +0	-1 +0	0 +1
Pair i -1	no -1	no -1	has -1	has -1
Output	$C_i=1$ $U_i=-1$	$C_i=0$ $U_i=-1$	$C_i=-1$ $U_i=1$	$C_i=0$ $U_i=1$

Rules for adding sign-digit numbers:

$Sum_i = C_{i-1} + U_i$

PRIOR ART

FIG. 6



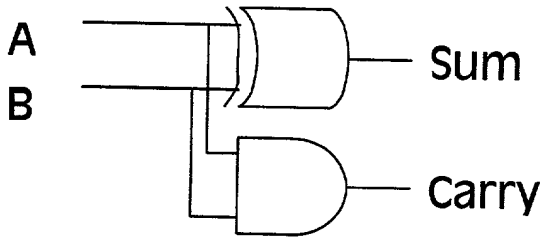


FIG. 7a

FIG. 7b

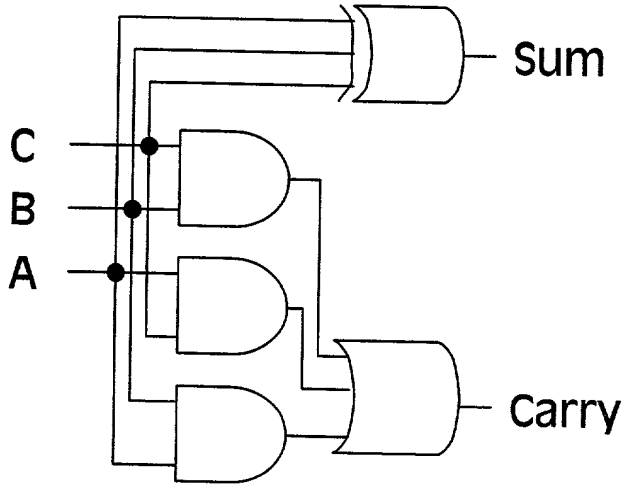
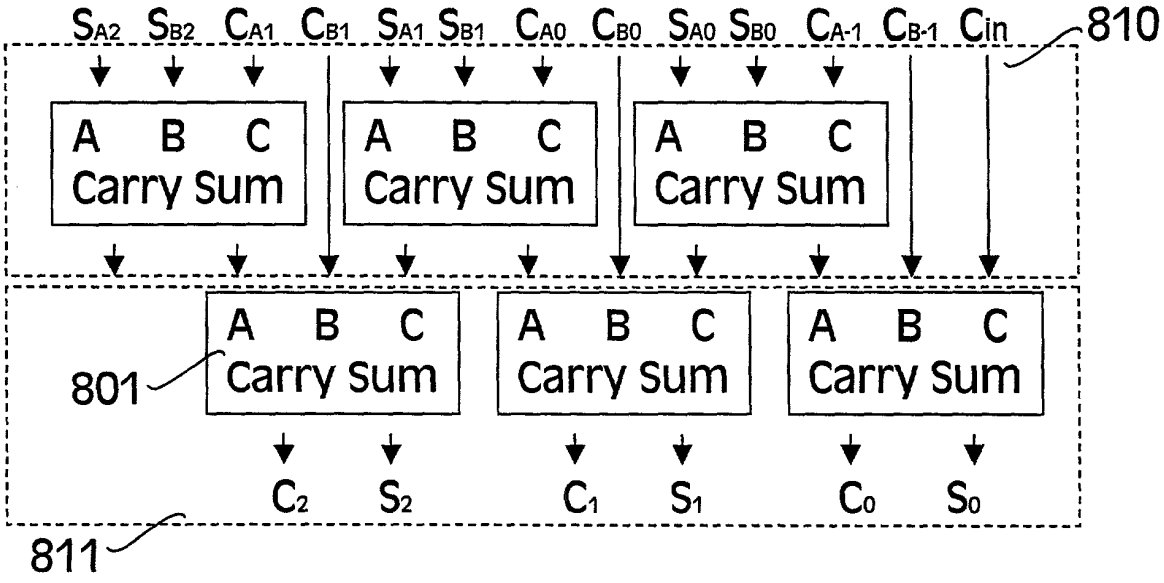


FIG. 7c

3:2 Compressor

ROM Address			ROM Data	
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1
A	B	C	Carry	Sum

FIG. 8



	C_2S_2	C_1S_1	C_0S_0
910	00	00	00
911	01	01	10
912	01	10	00
913	00	11	10
914	10	00	00
915	11	01	10
916	11	10	00
917	10	11	10

FIG. 9a

	C_2S_2	C_1S_1	C_0S_0
920	11	11	11
921	10	10	01
922	10	01	11
923	11	00	01
924	01	11	11
925	00	10	01
926	00	01	11
927	01	00	01

FIG. 9b

	C_2S_2	C_1S_1	C_0S_0		$\overline{C_2S_2}$	$\overline{C_1S_1}$	$\overline{C_0S_0}$	
3 =	00	01	01	→	11	10	10	= 2
2 =	00	01	00	→	11	10	11	= 3
1 =	00	00	01	→	11	11	10	= -4
0 =	00	00	00	→	11	11	11	= -3
-1 =	01	01	01	→	10	10	10	= -2
-2 =	01	01	00	→	10	10	11	= -1
-3 =	01	00	01	→	10	11	10	= 0
-4 =	01	00	00	→	10	11	11	= 1

$N \rightarrow \overline{N} = -N-3 \pmod 8$

FIG. 10

FIG. 11

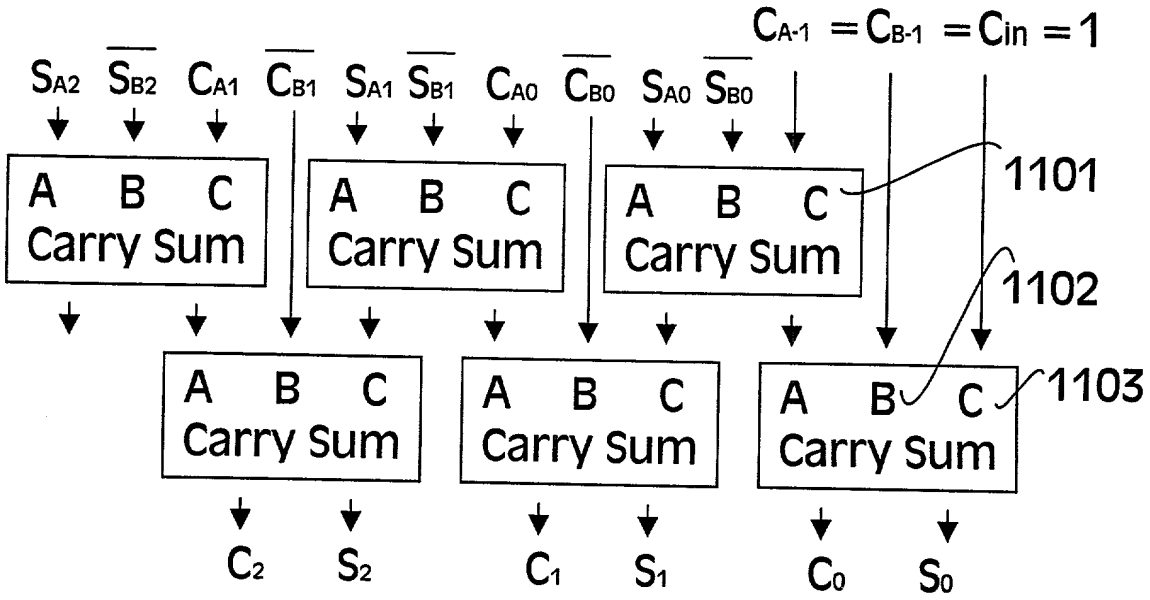

$C_{A-1} = C_{B-1} = C_{in} = 1$
S_{A2} $\overline{S_{B2}}$ C_{A1} $\overline{C_{B1}}$ S_{A1} $\overline{S_{B1}}$ C_{A0} $\overline{C_{B0}}$ S_{A0} $\overline{S_{B0}}$
A B C Carry Sum
1101
1102
1103
C_2 S_2 C_1 S_1 C_0 S_0

FIG. 12

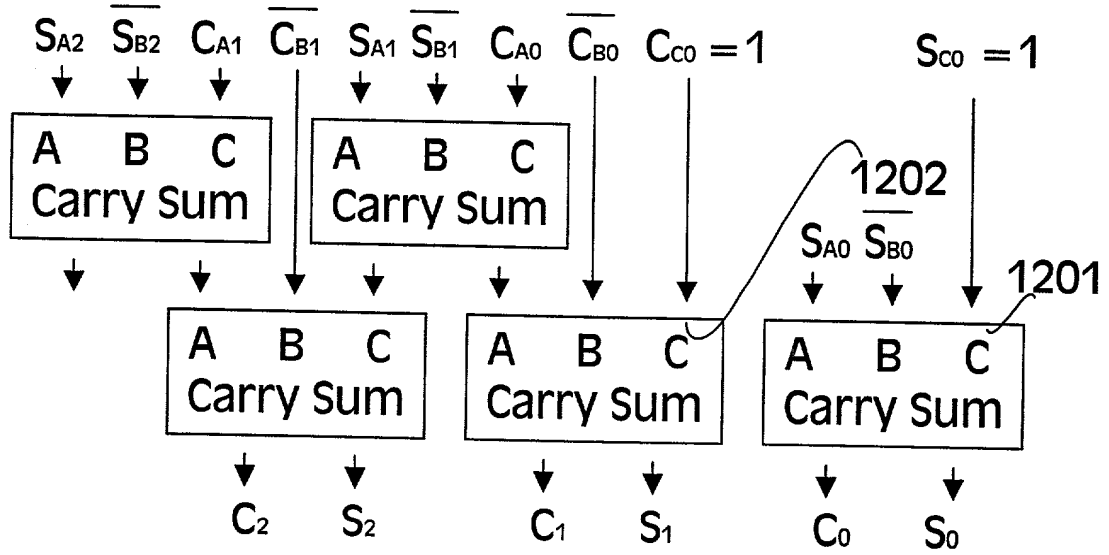
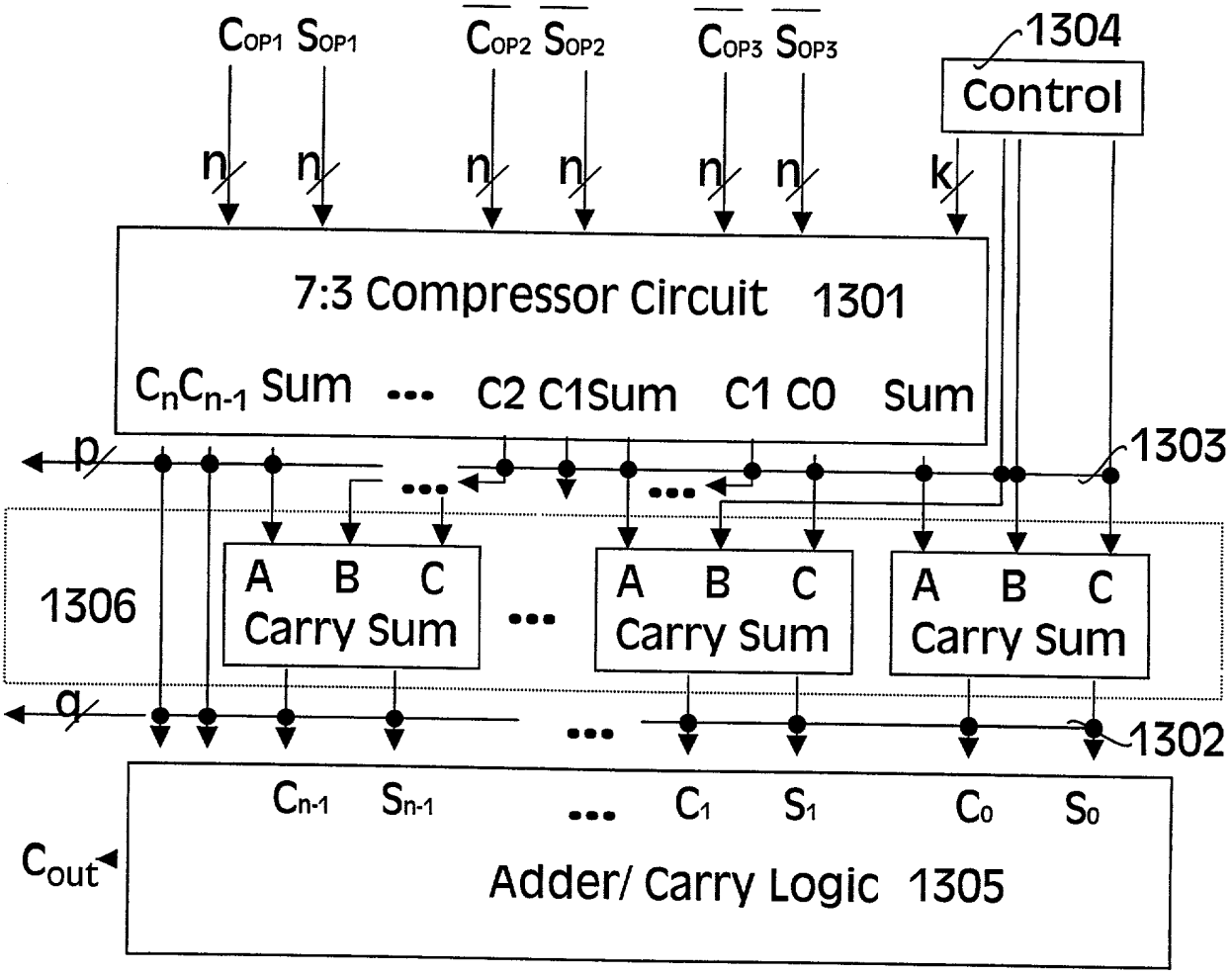

S_{A2} $\overline{S_{B2}}$ C_{A1} $\overline{C_{B1}}$ S_{A1} $\overline{S_{B1}}$ C_{A0} $\overline{C_{B0}}$ $C_{C0} = 1$
$S_{C0} = 1$
A B C Carry Sum
1202
S_{A0} $\overline{S_{B0}}$
1201
C_2 S_2 C_1 S_1 C_0 S_0

FIG. 13a


C_{OP1} S_{OP1}
$\overline{C_{OP2}}$ $\overline{S_{OP2}}$
$\overline{C_{OP3}}$ $\overline{S_{OP3}}$
1304
Control
n
k
7:3 Compressor Circuit 1301
C_nC_{n-1} Sum ... C2 C1Sum C1 C0 Sum
p
1303
1306
A B C
Carry Sum
q
1302
C_{n-1} S_{n-1} ... C_1 S_1 C_0 S_0
C_{out}
Adder/ Carry Logic 1305

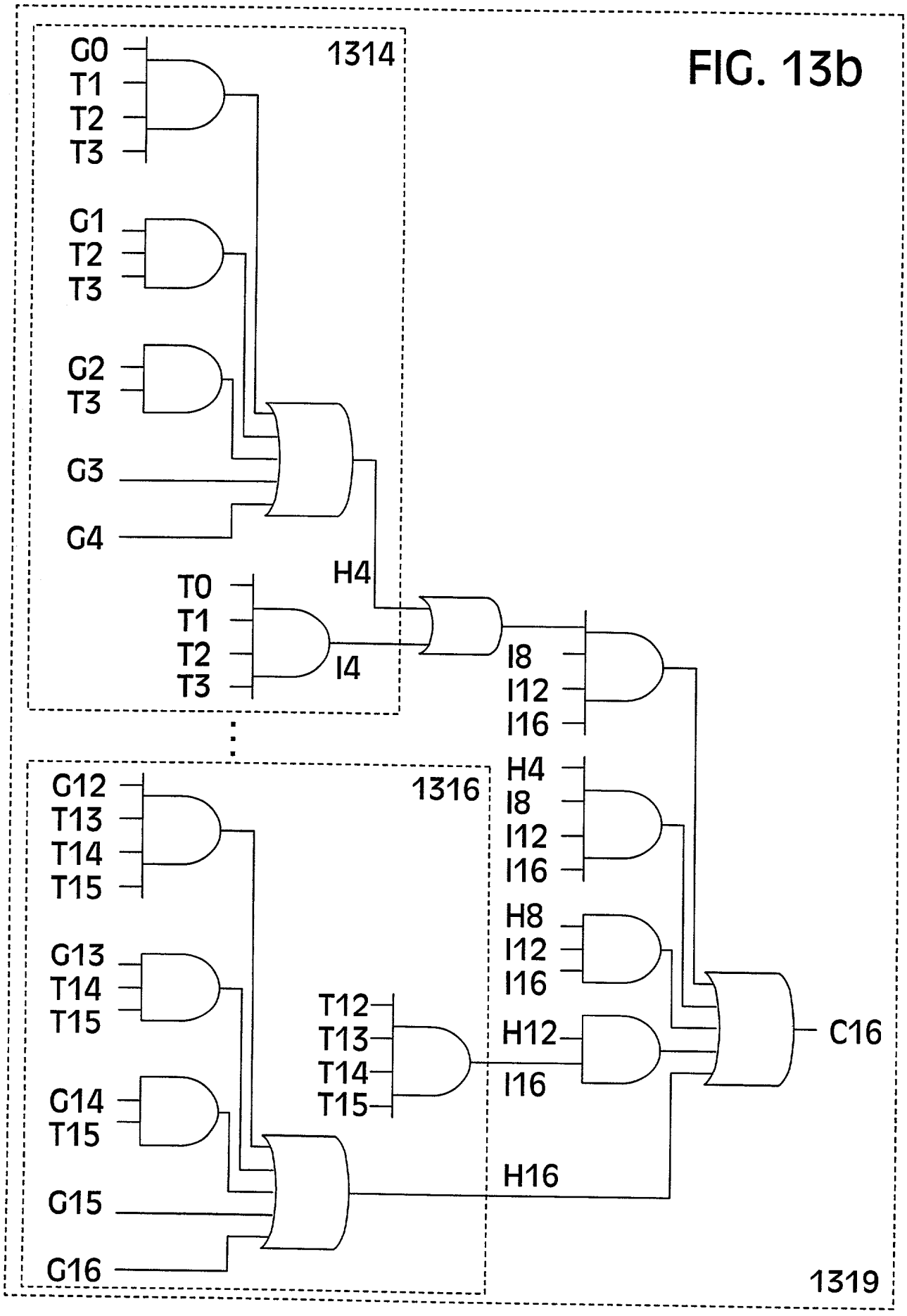
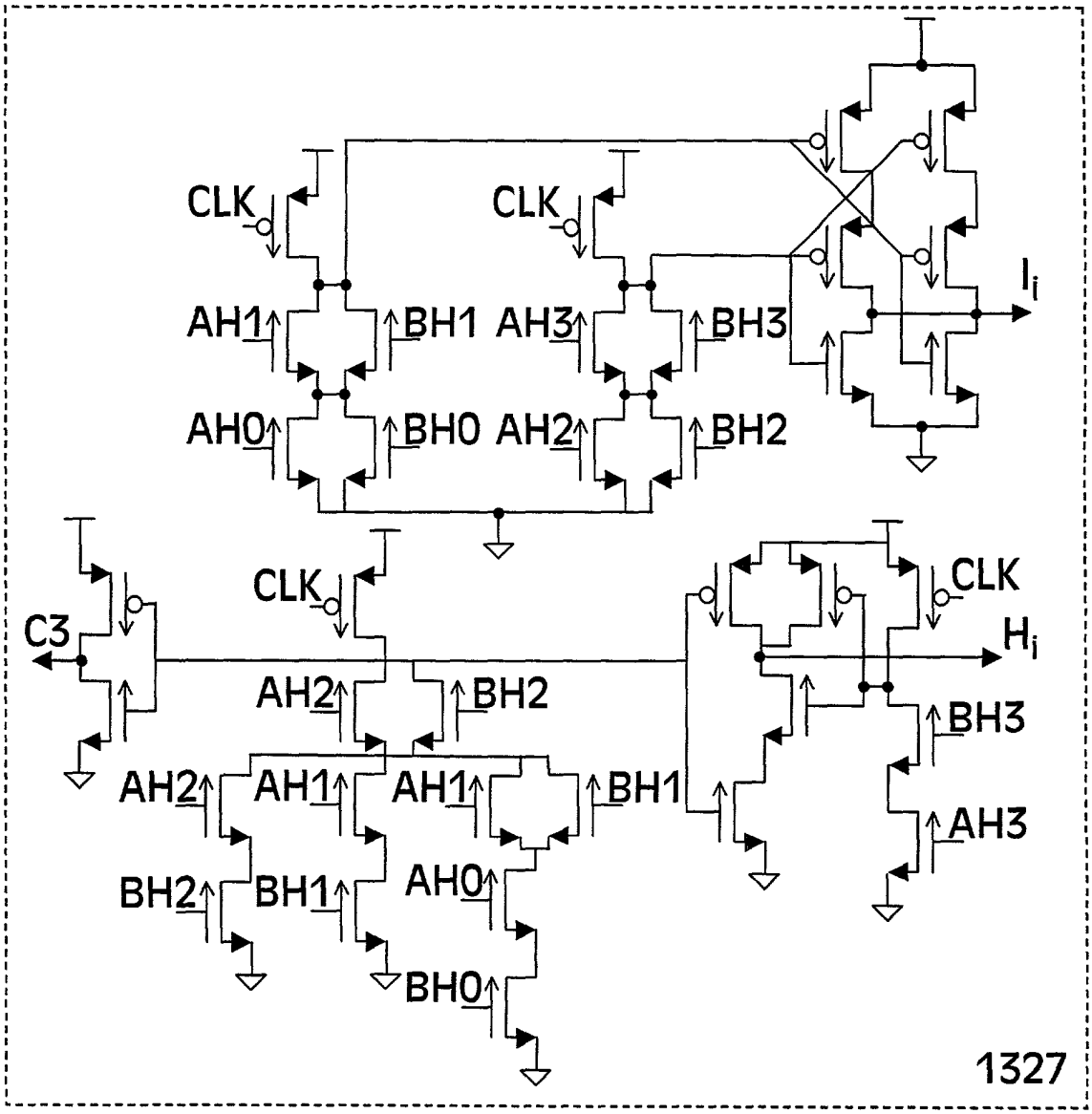

1314
G0
T1
T2
T3
G1
T2
T3
G2
T3
G3
G4
T0
T1
T2
T3
I4
H4
I8
I12
I16
1316
G12
T13
T14
T15
G13
T14
T15
G14
T15
G15
G16
T12
T13
T14
T15
H4
I8
I12
I16
H8
I12
I16
H12
I16
H16
C16
1319

FIG. 13b

FIG. 13c



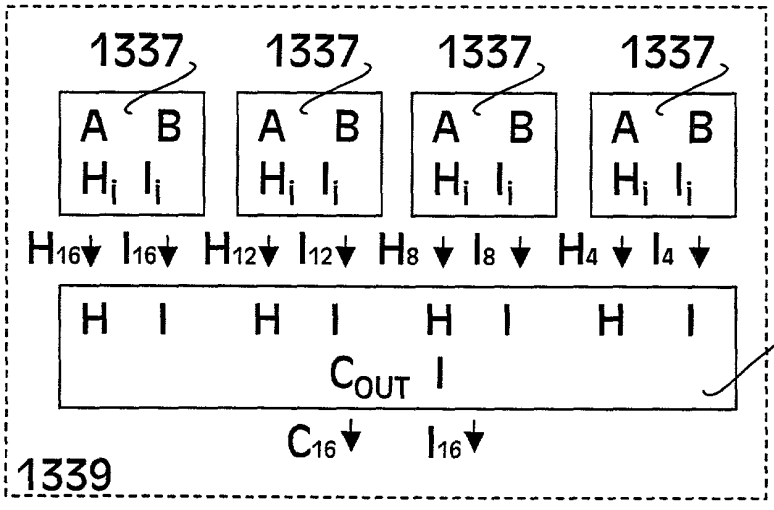


FIG. 13d

FIG. 13e

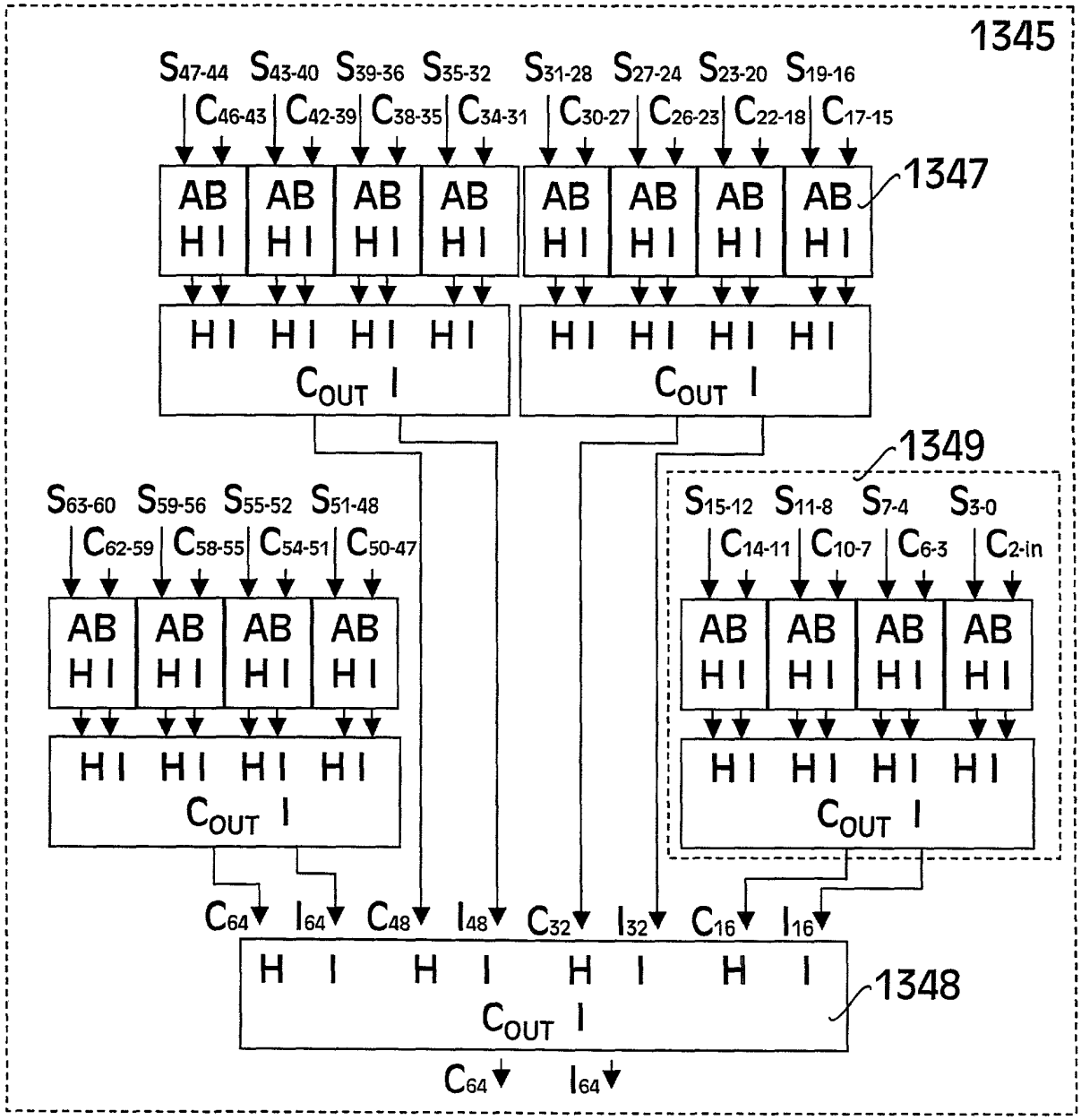

1345
S47-44 S43-40 S39-36 S35-32 S31-28 S27-24 S23-20 S19-16
C46-43 C42-39 C38-35 C34-31 C30-27 C26-23 C22-18 C17-15
1347
AB HI
HI HI HI HI
COUT I
1349
S63-60 S59-56 S55-52 S51-48
C62-59 C58-55 C54-51 C50-47
S15-12 S11-8 S7-4 S3-0
C14-11 C10-7 C6-3 C2-in
C64 I64 C48 I48 C32 I32 C16 I16
H I
1348

FIG. 14

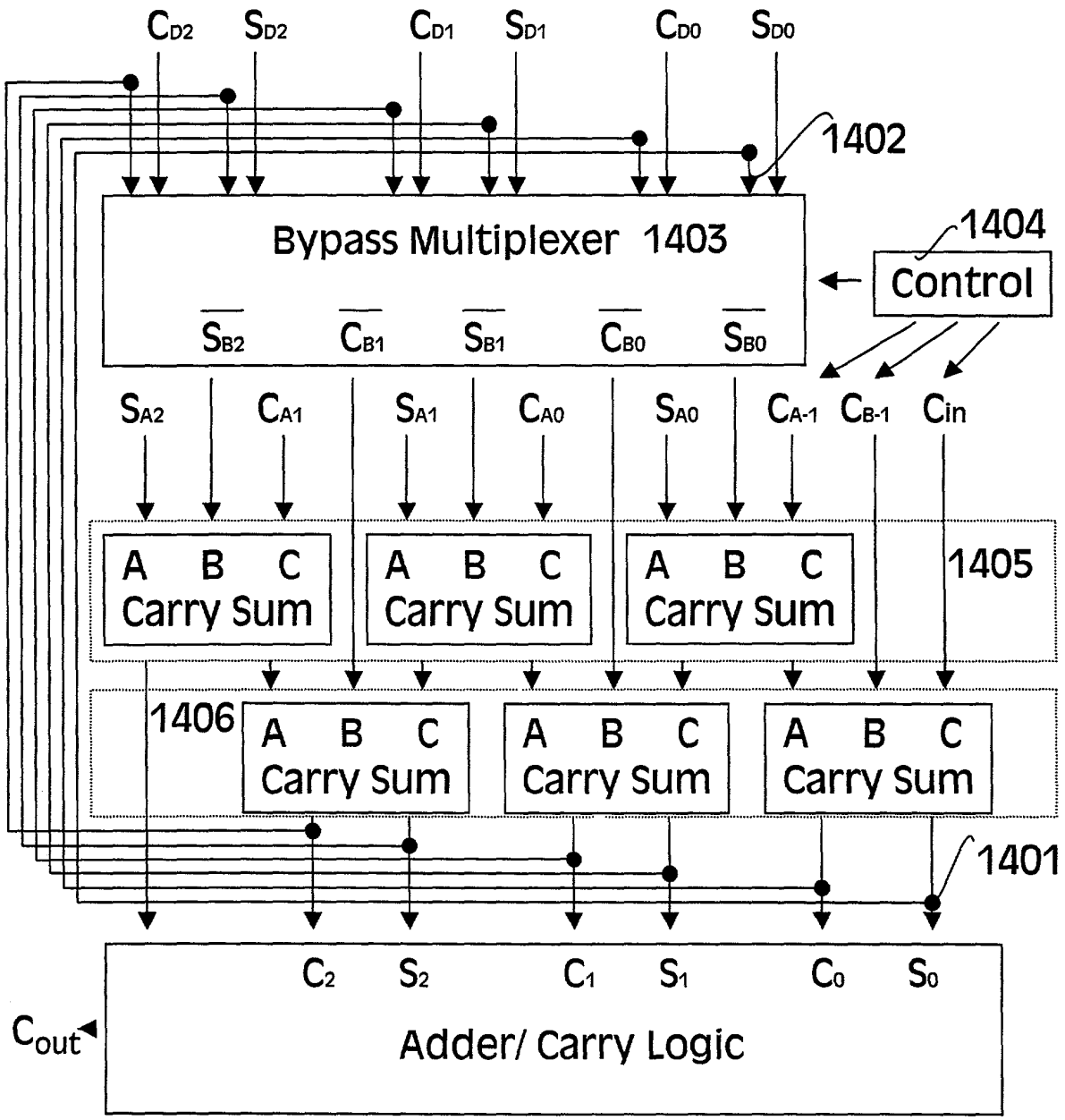

C_{D2} S_{D2} C_{D1} S_{D1} C_{D0} S_{D0}
1402
Bypass Multiplexer 1403
1404
Control
$\overline{S_{B2}}$ $\overline{C_{B1}}$ $\overline{S_{B1}}$ $\overline{C_{B0}}$ $\overline{S_{B0}}$
S_{A2} C_{A1} S_{A1} C_{A0} S_{A0} C_{A-1} C_{B-1} Cin
A B C Carry Sum
1405
1406
C_2 S_2 C_1 S_1 C_0 S_0
1401
C_{out}
Adder/ Carry Logic

FIG. 15

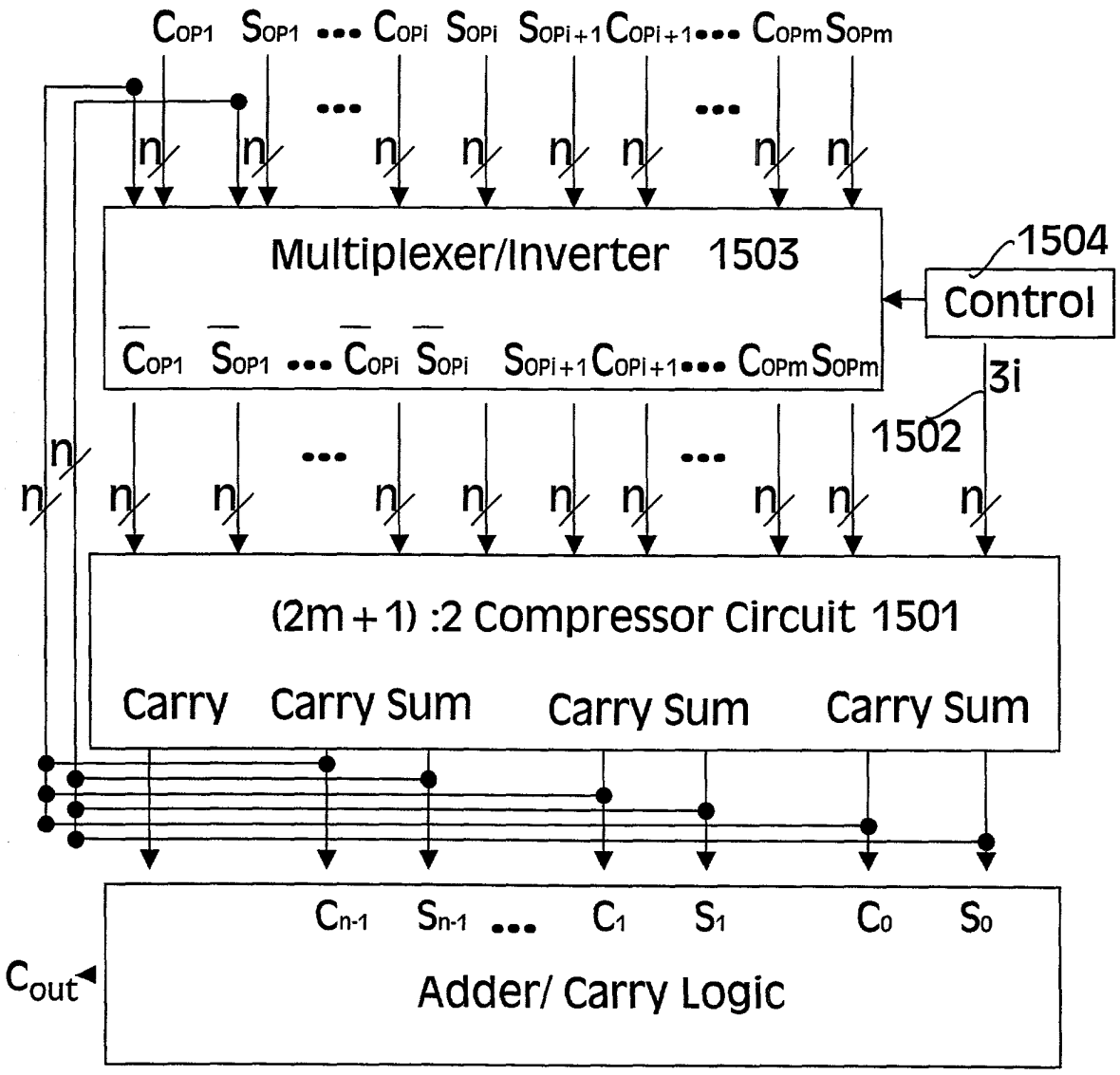

COP1 SOP1 ••• COPi SOPi SOPi+1 COPi+1 ••• COPm SOPm
n
Multiplexer/Inverter 1503
1504
Control
COP1 SOP1 ••• COPi SOPi SOPi+1 COPi+1 ••• COPm SOPm
3i
1502
(2m+1) :2 Compressor Circuit 1501
Carry
Carry Sum
Carry Sum
Carry Sum
Cn-1 Sn-1 ••• C1 S1 C0 S0
Cout
Adder/ Carry Logic

FIG. 16a

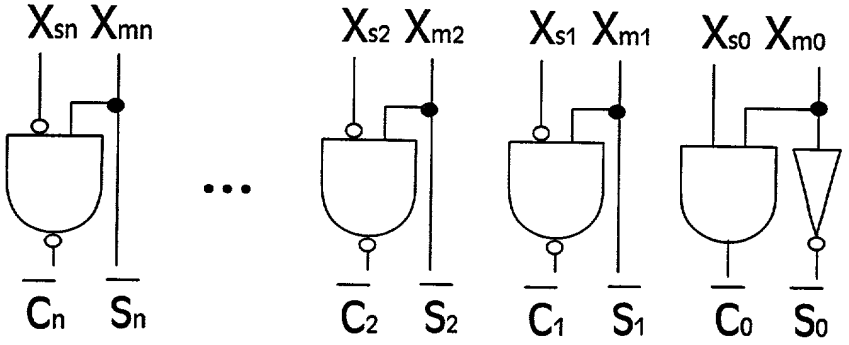


FIG. 16b

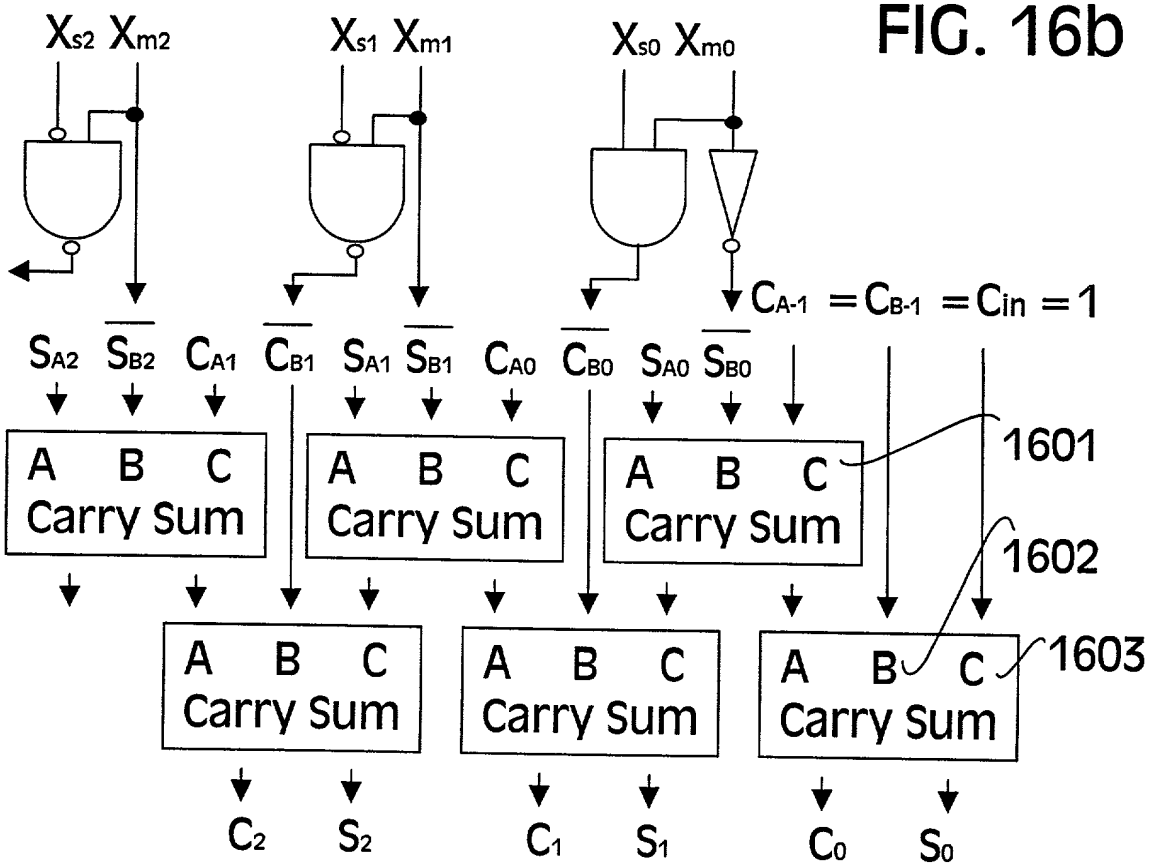
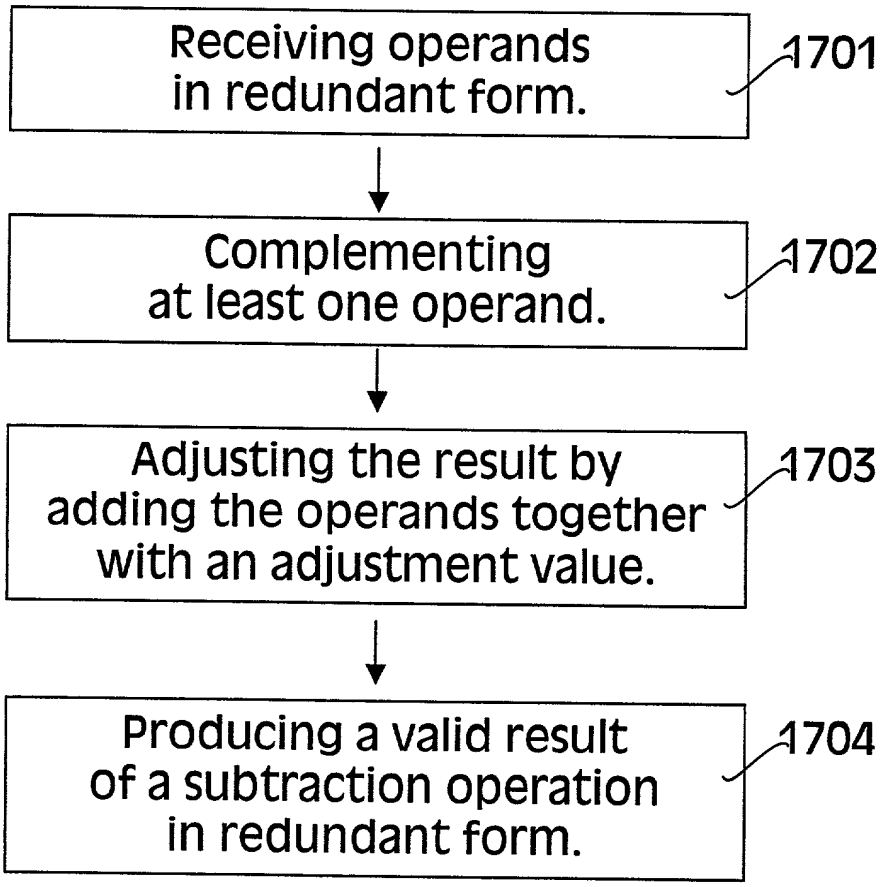


FIG. 17


Receiving operands in redundant form.
1701
Complementing at least one operand.
1702
Adjusting the result by adding the operands together with an adjustment value.
1703
Producing a valid result of a subtraction operation in redundant form.
1704

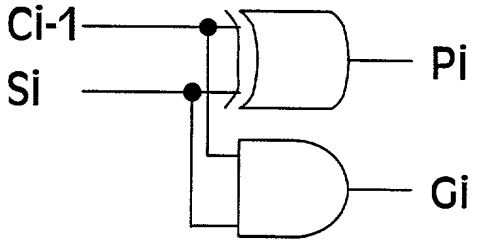
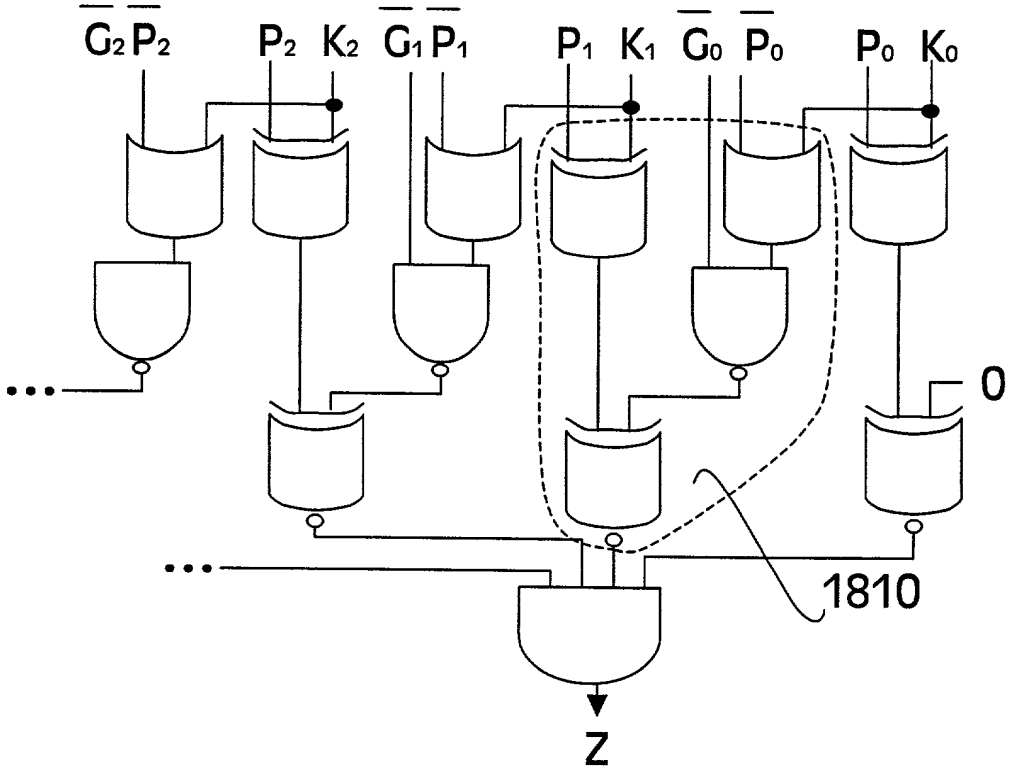


FIG. 18a

FIG. 18b



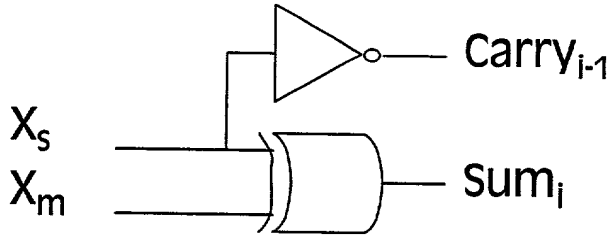


FIG. 19a

FIG. 19b

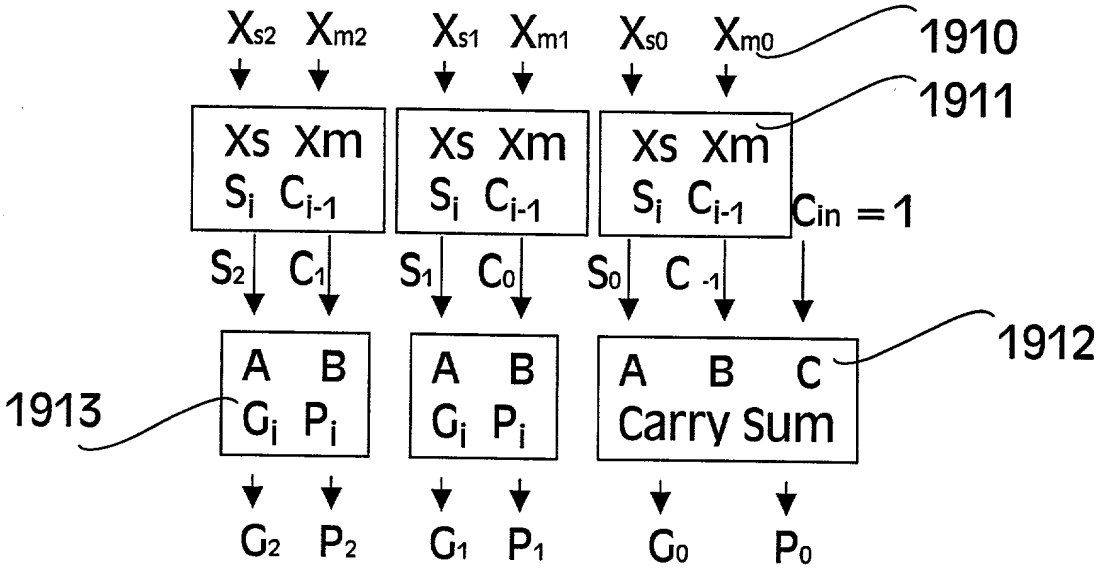


FIG. 20

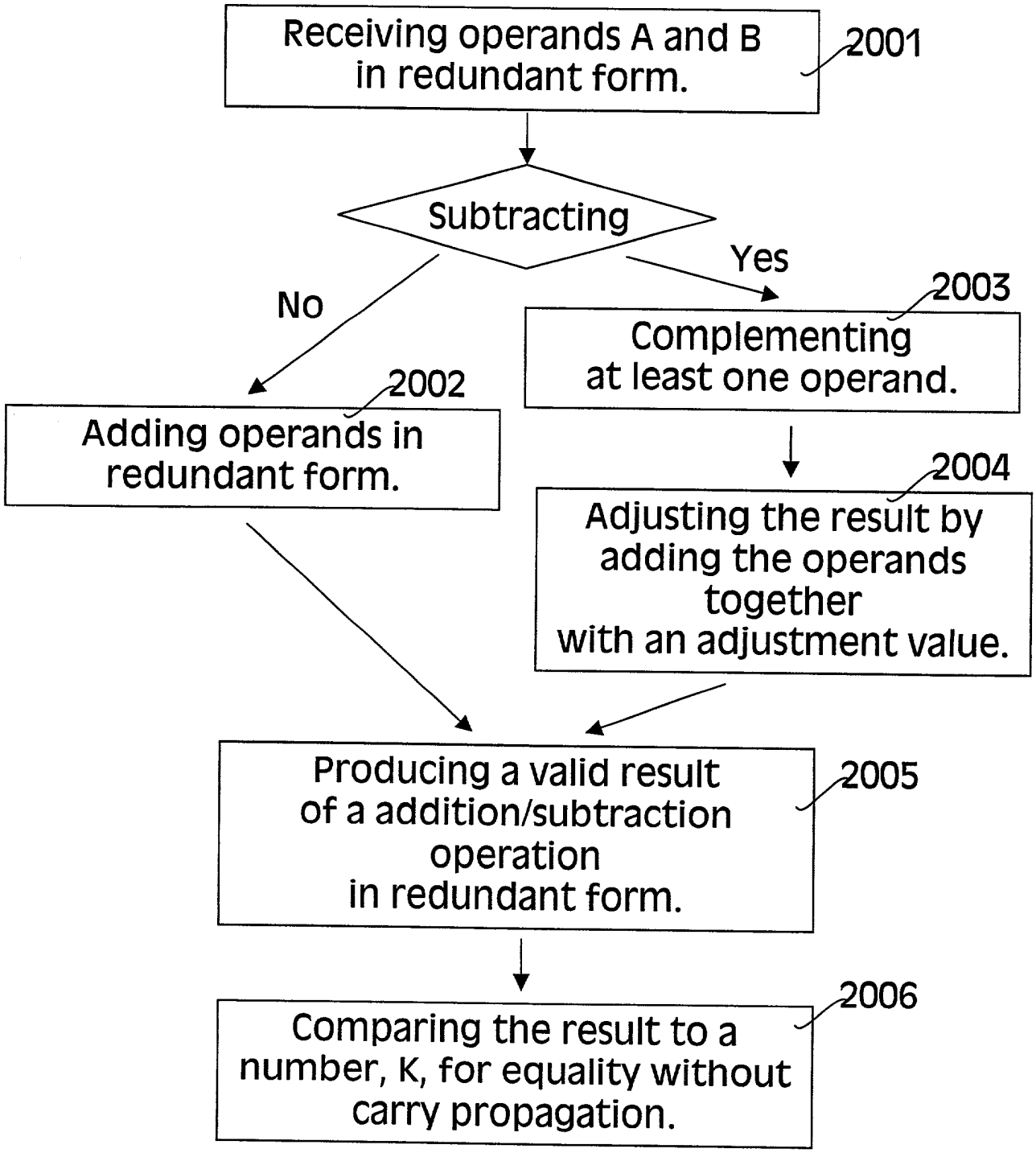

Receiving operands A and B in redundant form.
2001
Subtracting
Yes
No
2003
Complementing at least one operand.
2002
Adding operands in redundant form.
2004
Adjusting the result by adding the operands together with an adjustment value.
Producing a valid result of a addition/subtraction operation in redundant form.
2005
Comparing the result to a number, K, for equality without carry propagation.
2006

FIG. 21a

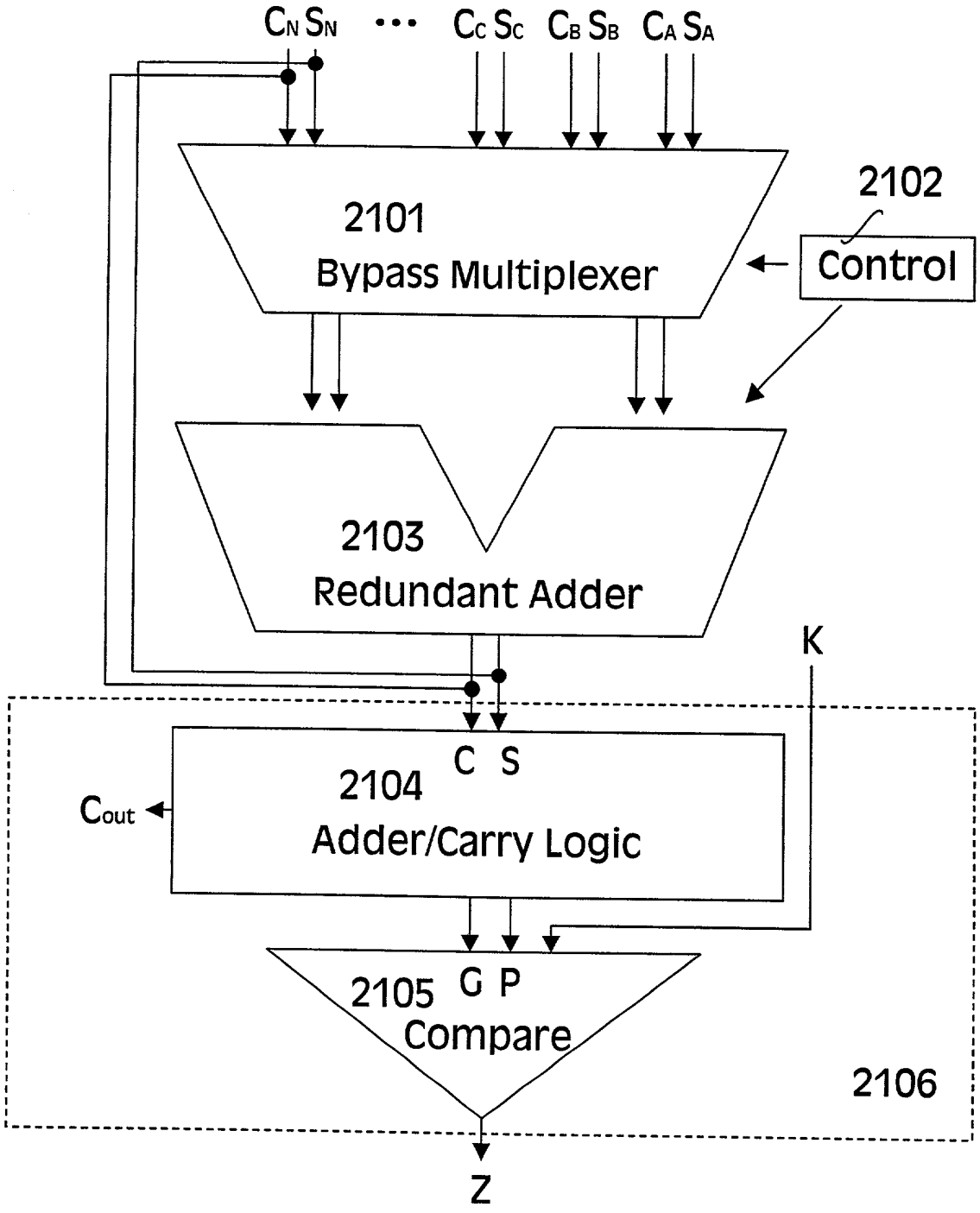

C_N S_N ••• C_C S_C C_B S_B C_A S_A
2101
Bypass Multiplexer
2102
Control
2103
Redundant Adder
K
C S
2104
Adder/Carry Logic
C_{out}
2105 G P
Compare
2106
Z

FIG. 21b

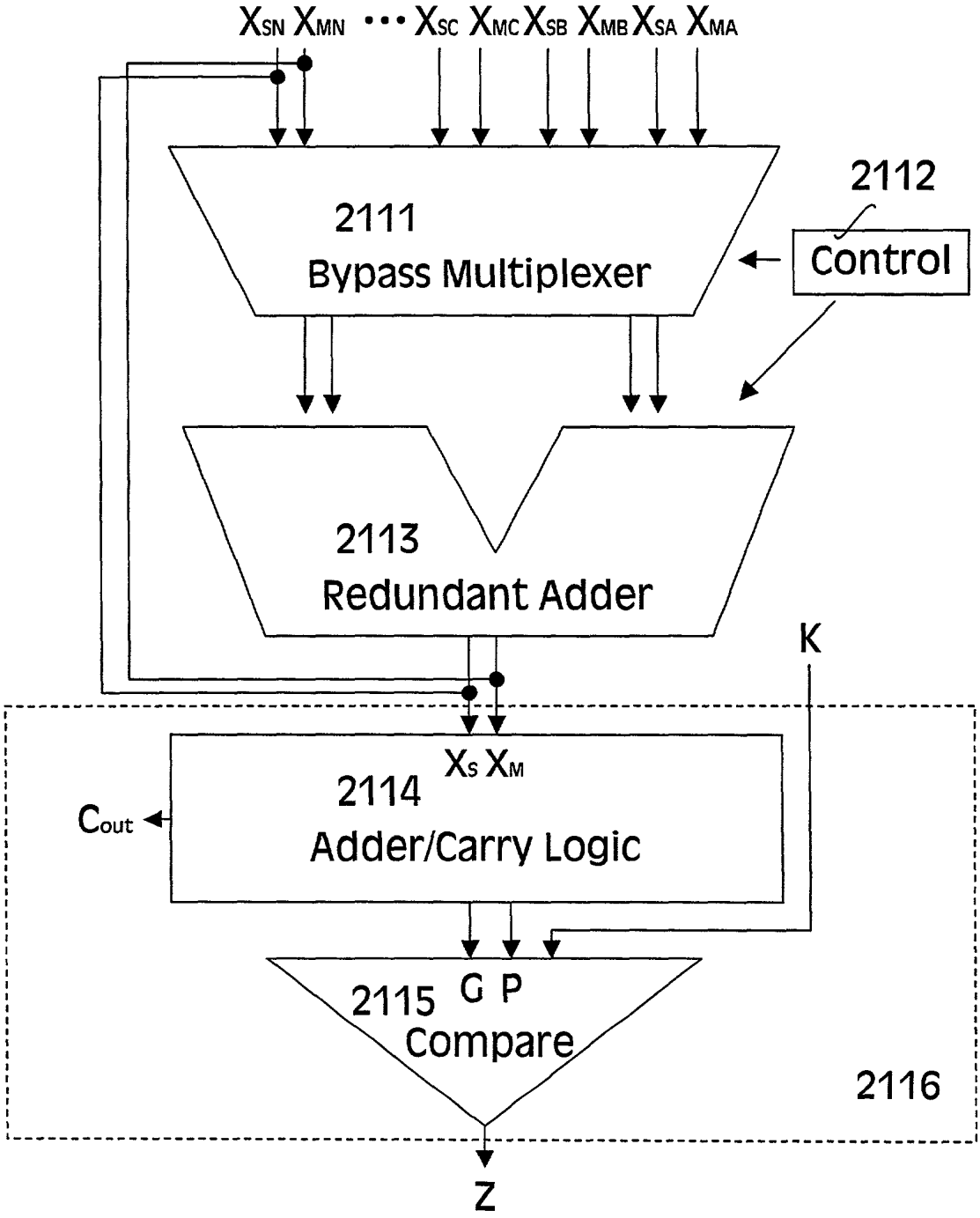

X_{SN} X_{MN} ••• X_{SC} X_{MC} X_{SB} X_{MB} X_{SA} X_{MA}
2111
Bypass Multiplexer
2112
Control
2113
Redundant Adder
K
X_S X_M
2114
Adder/Carry Logic
C_{out}
2115 G P
Compare
2116
Z

FIG. 22a

C_2S_2	C_1S_1	C_0S_0
00	00	00
01	01	10
01	10	00
00	11	10
10	00	00
11	01	10
11	10	00
10	11	10

$(S_2 \oplus C_1) \oplus (S_1 + C_0)$	
0 **0** 0 **0** 0 **0** 0	2200
1 **1** 0 **0** 1 **1** 1	2201
1 **0** 1 **0** 0 **0** 0	2202
0 **0** 1 **0** 1 **1** 1	2203
0 **0** 0 **0** 0 **0** 0	2204
1 **1** 0 **0** 1 **1** 1	2205
1 **0** 1 **0** 0 **0** 0	2206
0 **1** 1 **0** 1 **1** 1	2207

FIG. 22b

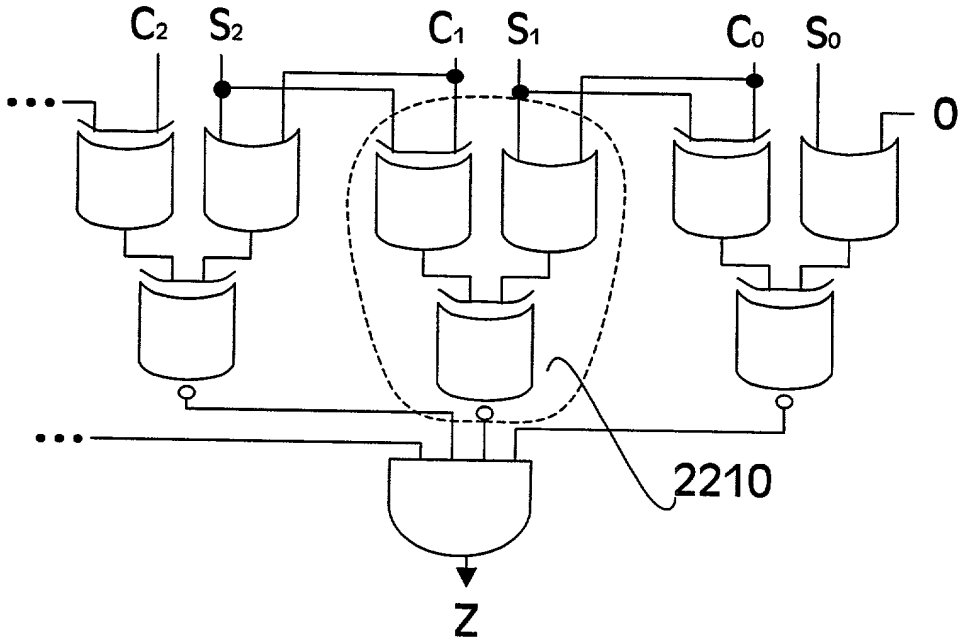


FIG. 22c

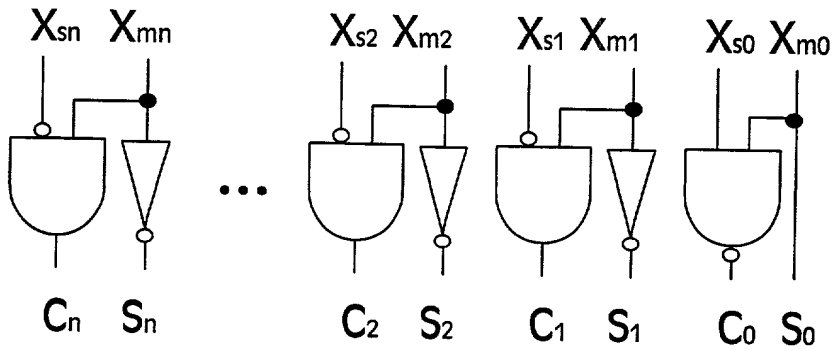


FIG. 22d

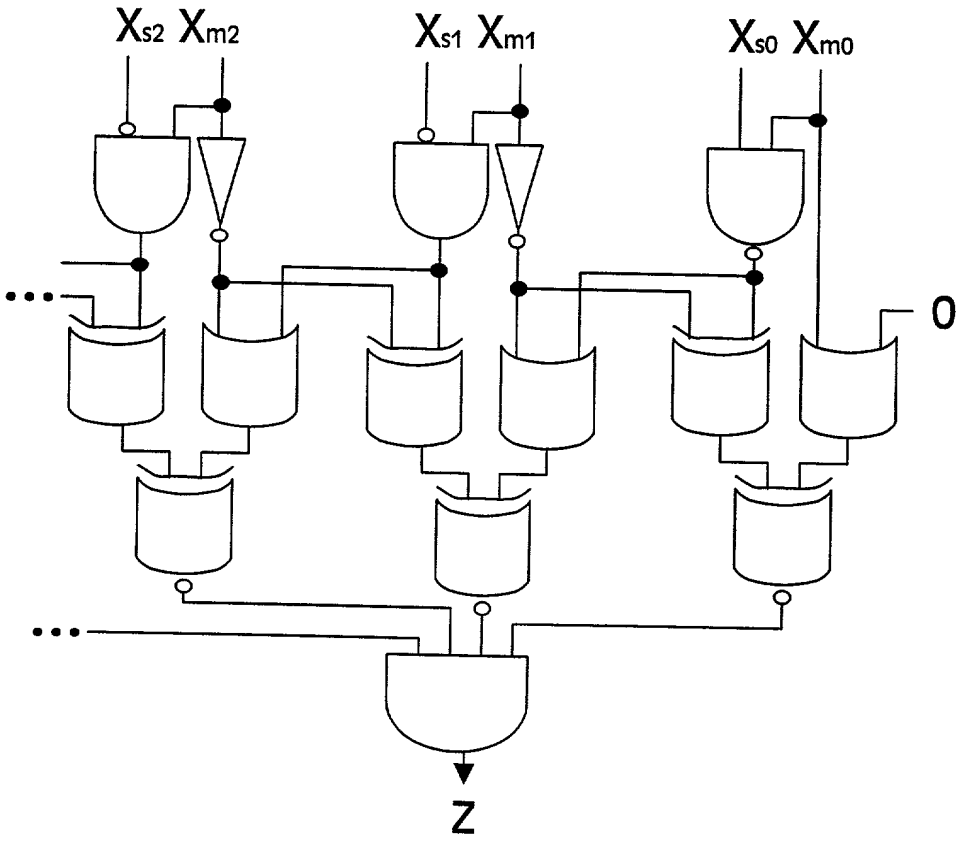


FIG. 23

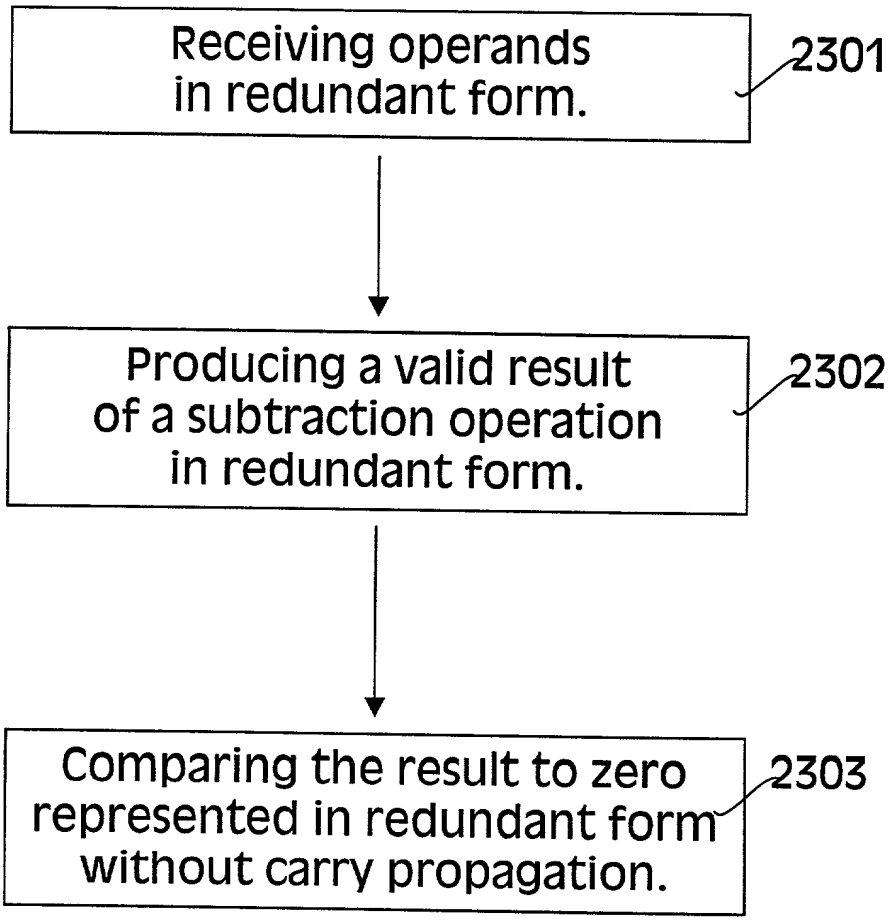

Receiving operands in redundant form.
2301
Producing a valid result of a subtraction operation in redundant form.
2302
Comparing the result to zero represented in redundant form without carry propagation.
2303

FIG. 24

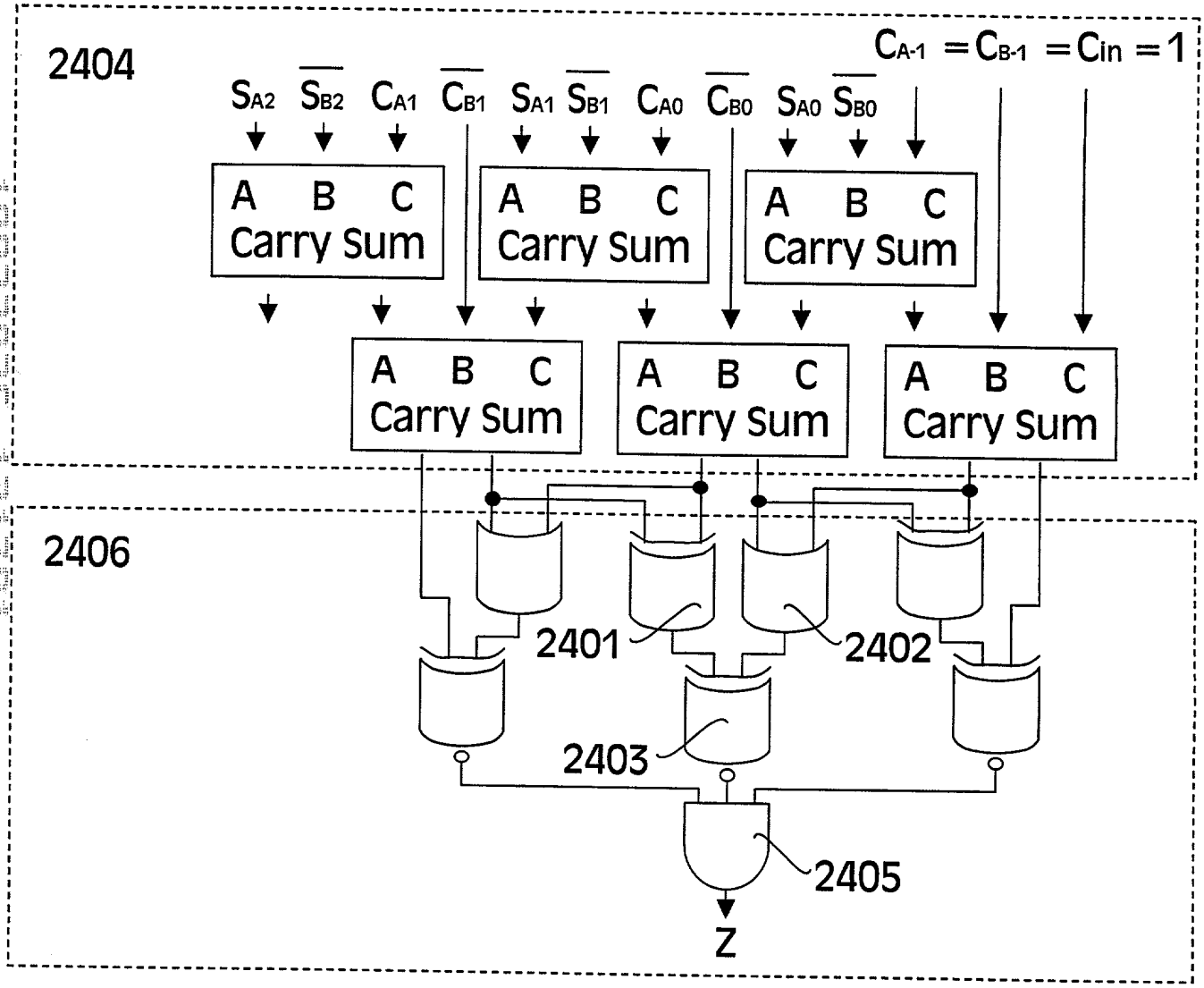

2404
$C_{A-1} = C_{B-1} = C_{in} = 1$
S_{A2} $\overline{S_{B2}}$ C_{A1} $\overline{C_{B1}}$ S_{A1} $\overline{S_{B1}}$ C_{A0} $\overline{C_{B0}}$ S_{A0} $\overline{S_{B0}}$
A B C Carry Sum
A B C Carry Sum
A B C Carry Sum
A B C Carry Sum
A B C Carry Sum
A B C Carry Sum
2406
2401
2402
2403
2405
Z

FIG. 25a

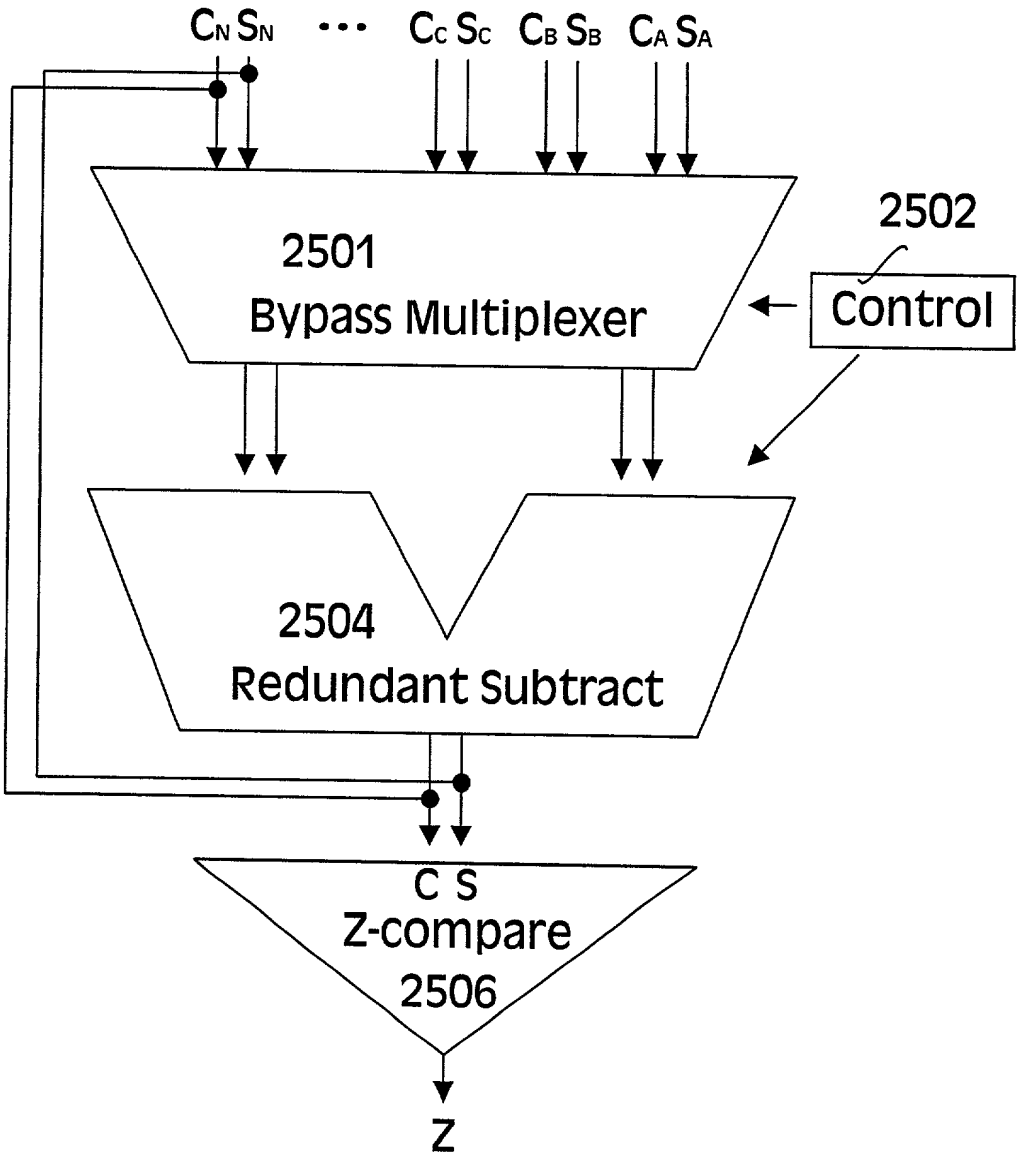

C_N S_N ... C_C S_C C_B S_B C_A S_A
2501
Bypass Multiplexer
2502
Control
2504
Redundant Subtract
C S
Z-compare
2506
Z

FIG. 25b

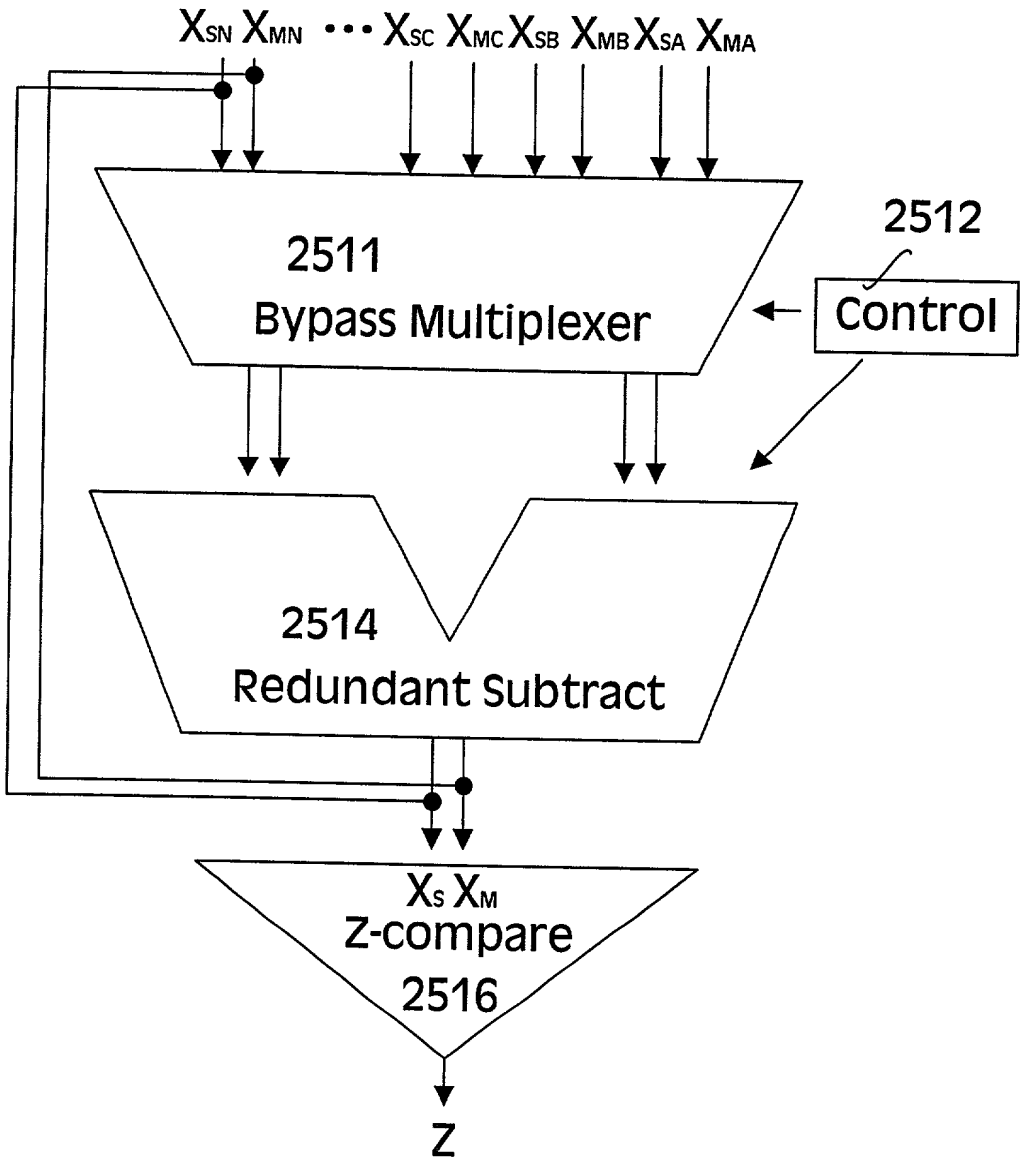

X_{SN} X_{MN} ••• X_{SC} X_{MC} X_{SB} X_{MB} X_{SA} X_{MA}
2511
Bypass Multiplexer
2512
Control
2514
Redundant Subtract
X_S X_M
Z-compare
2516
Z

FIG. 26

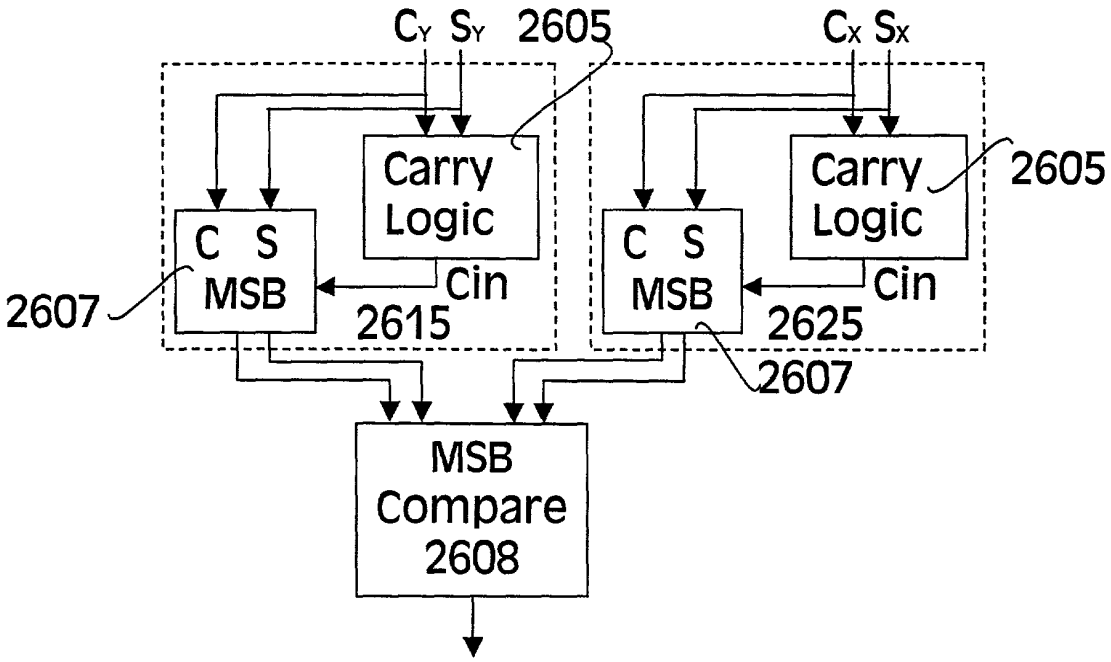

C_Y S_Y
2605
C_X S_X
Carry Logic
C S MSB
Cin
2615
2607
Carry Logic
2605
C S MSB
Cin
2625
2607
MSB Compare 2608

FIG. 27a

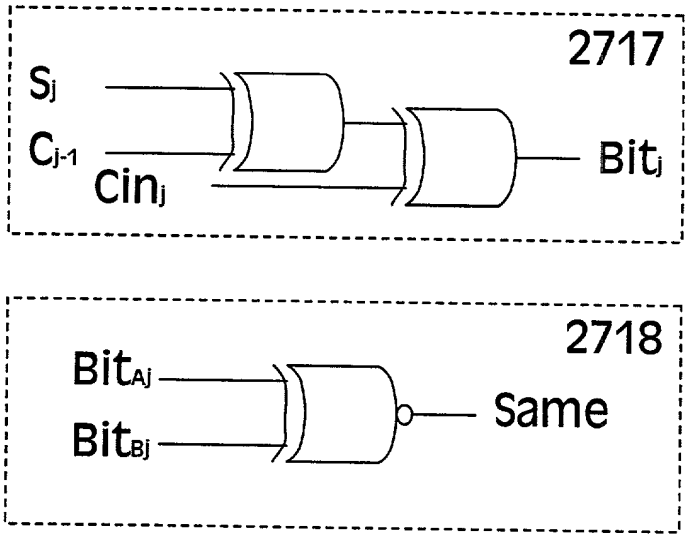


FIG. 27b

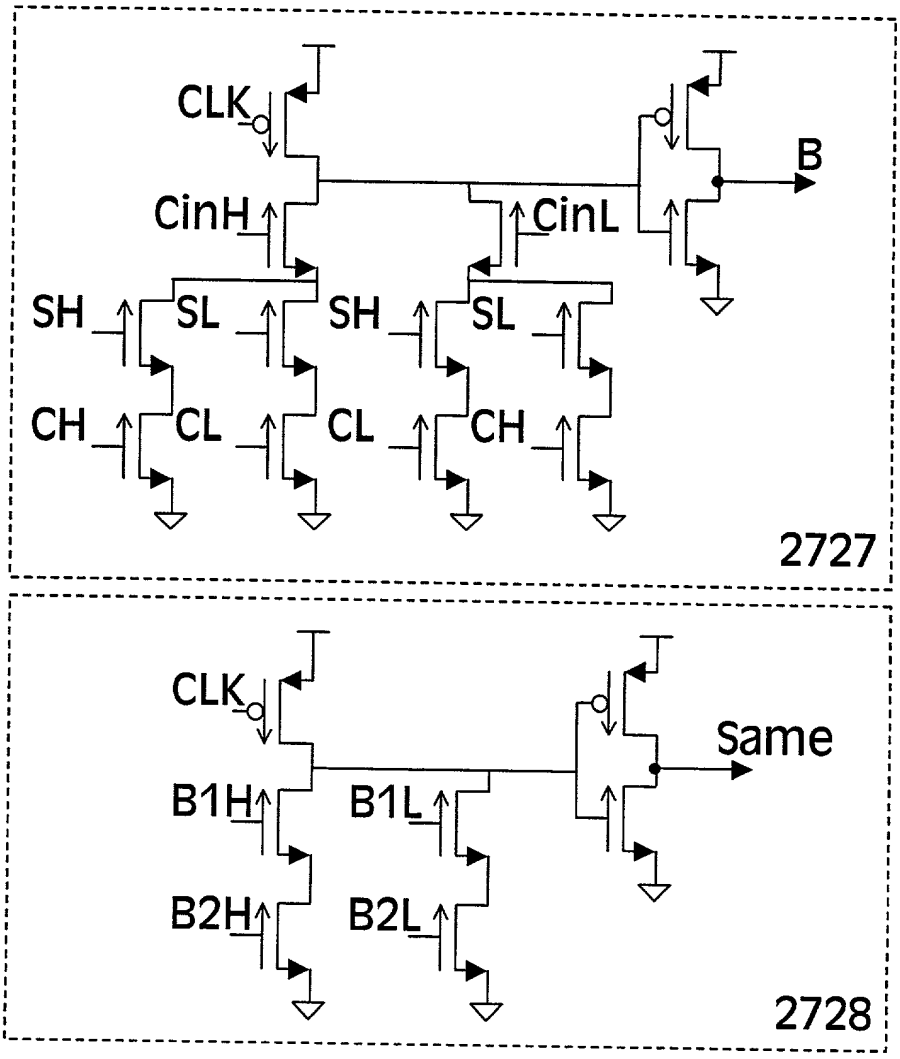


FIG. 28a

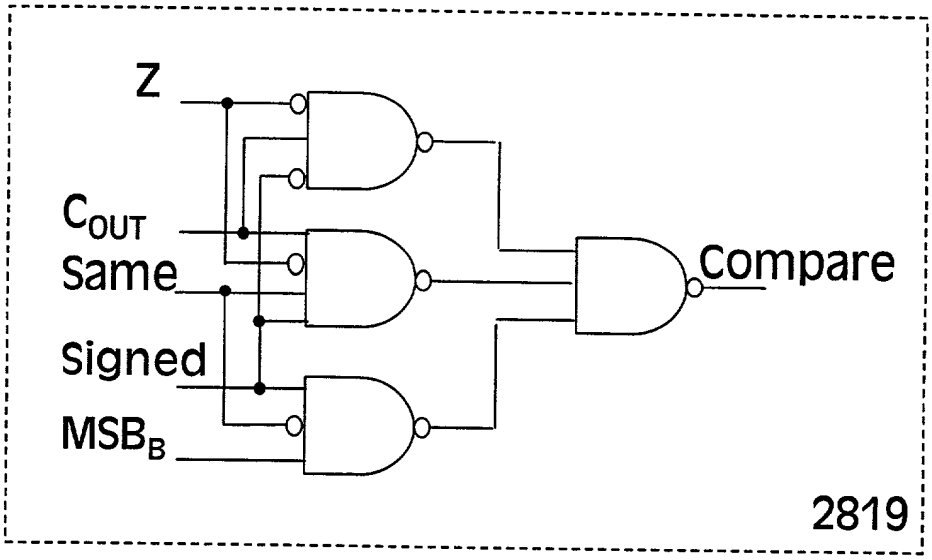


FIG. 28b

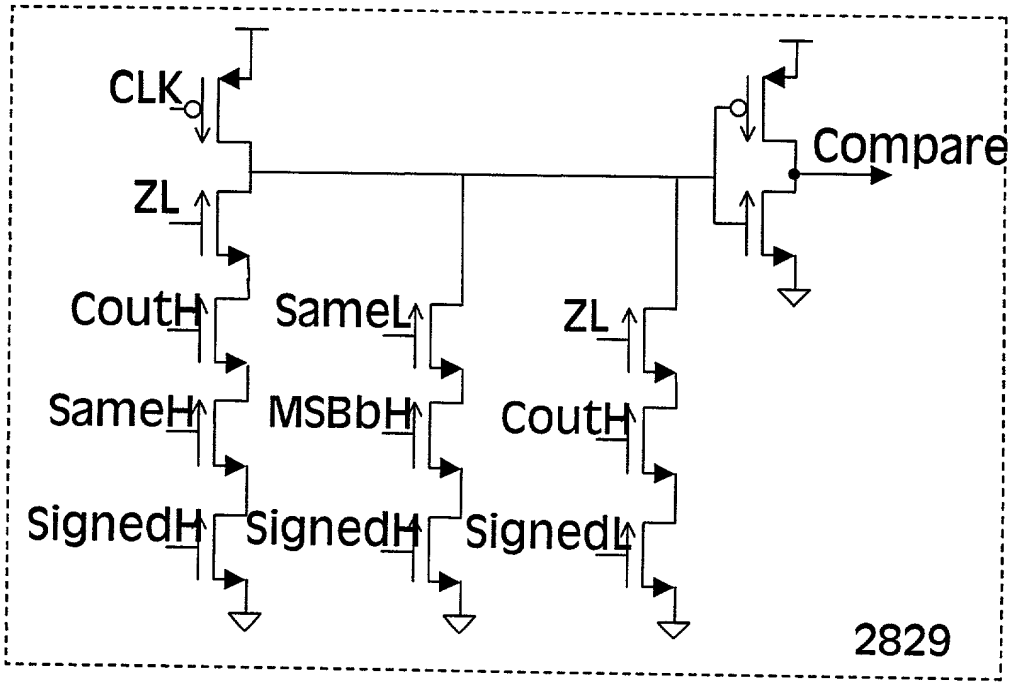


FIG. 29

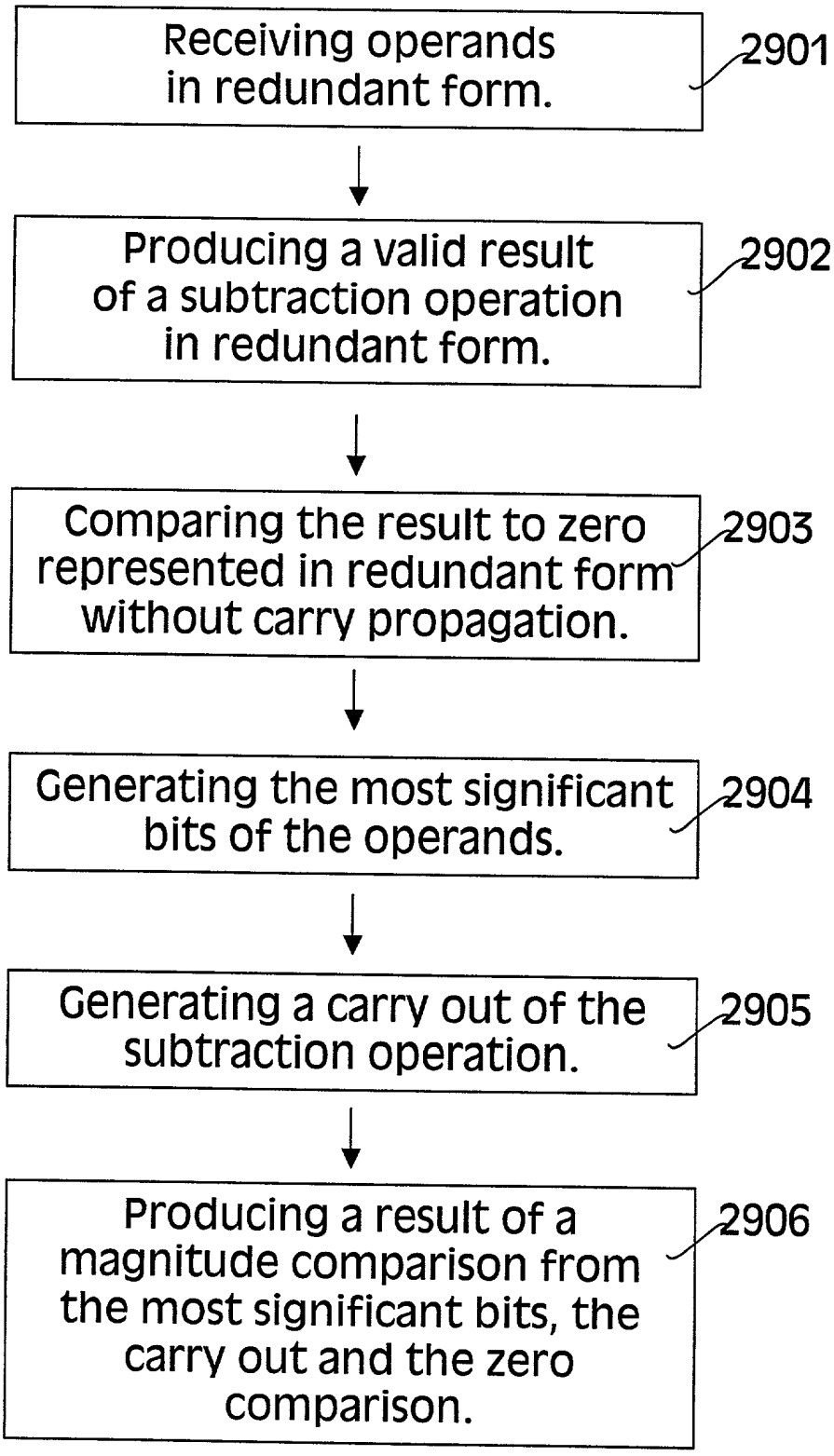

Receiving operands in redundant form.
2901
Producing a valid result of a subtraction operation in redundant form.
2902
Comparing the result to zero represented in redundant form without carry propagation.
2903
Generating the most significant bits of the operands.
2904
Generating a carry out of the subtraction operation.
2905
Producing a result of a magnitude comparison from the most significant bits, the carry out and the zero comparison.
2906

FIG. 30a

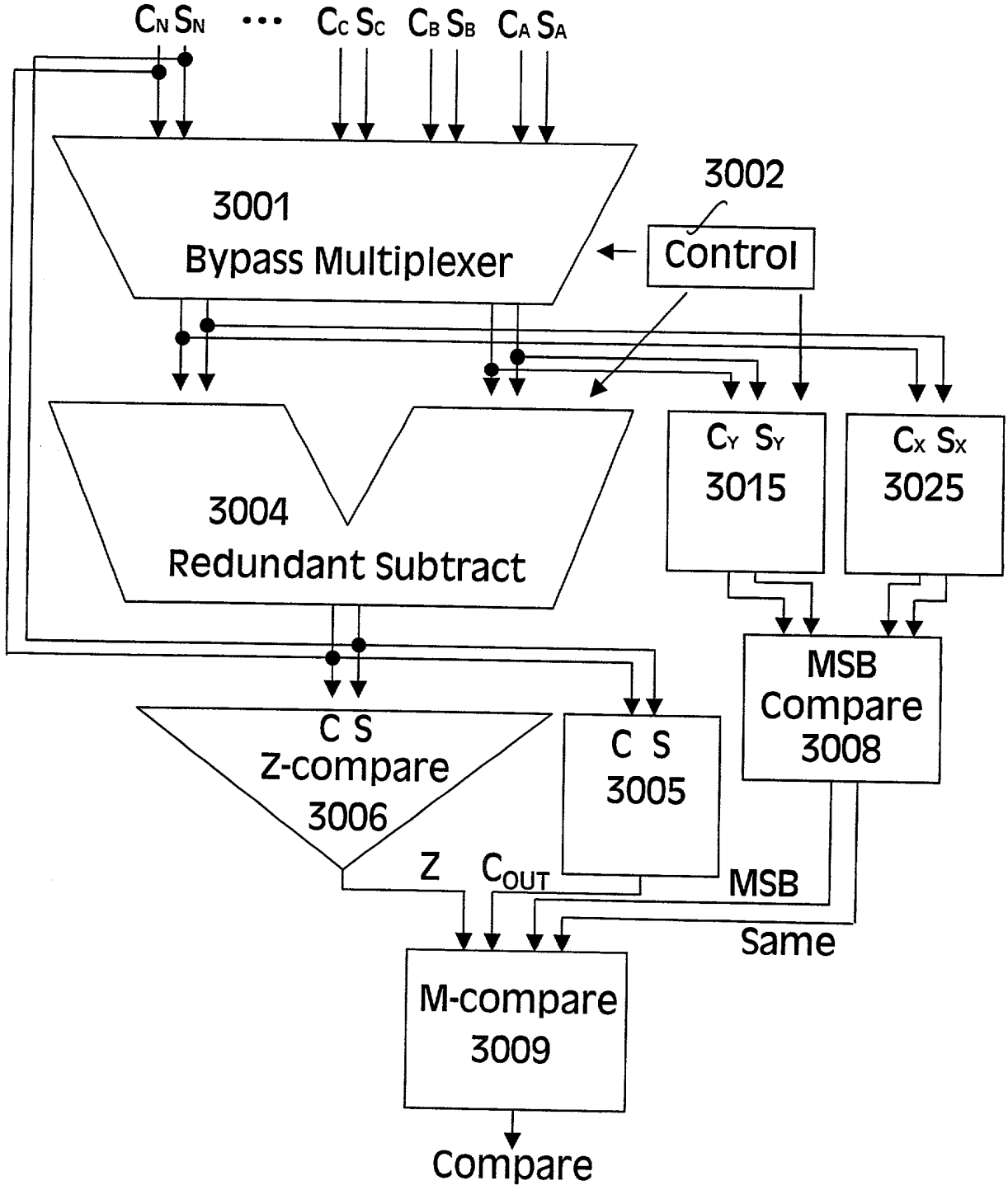

C_N S_N ... C_C S_C C_B S_B C_A S_A
3001
Bypass Multiplexer
3002
Control
3004
Redundant Subtract
C_Y S_Y
3015
C_X S_X
3025
MSB
Compare
3008
C S
Z-compare
3006
C S
3005
Z
C_{OUT}
MSB
Same
M-compare
3009
Compare

FIG. 30b

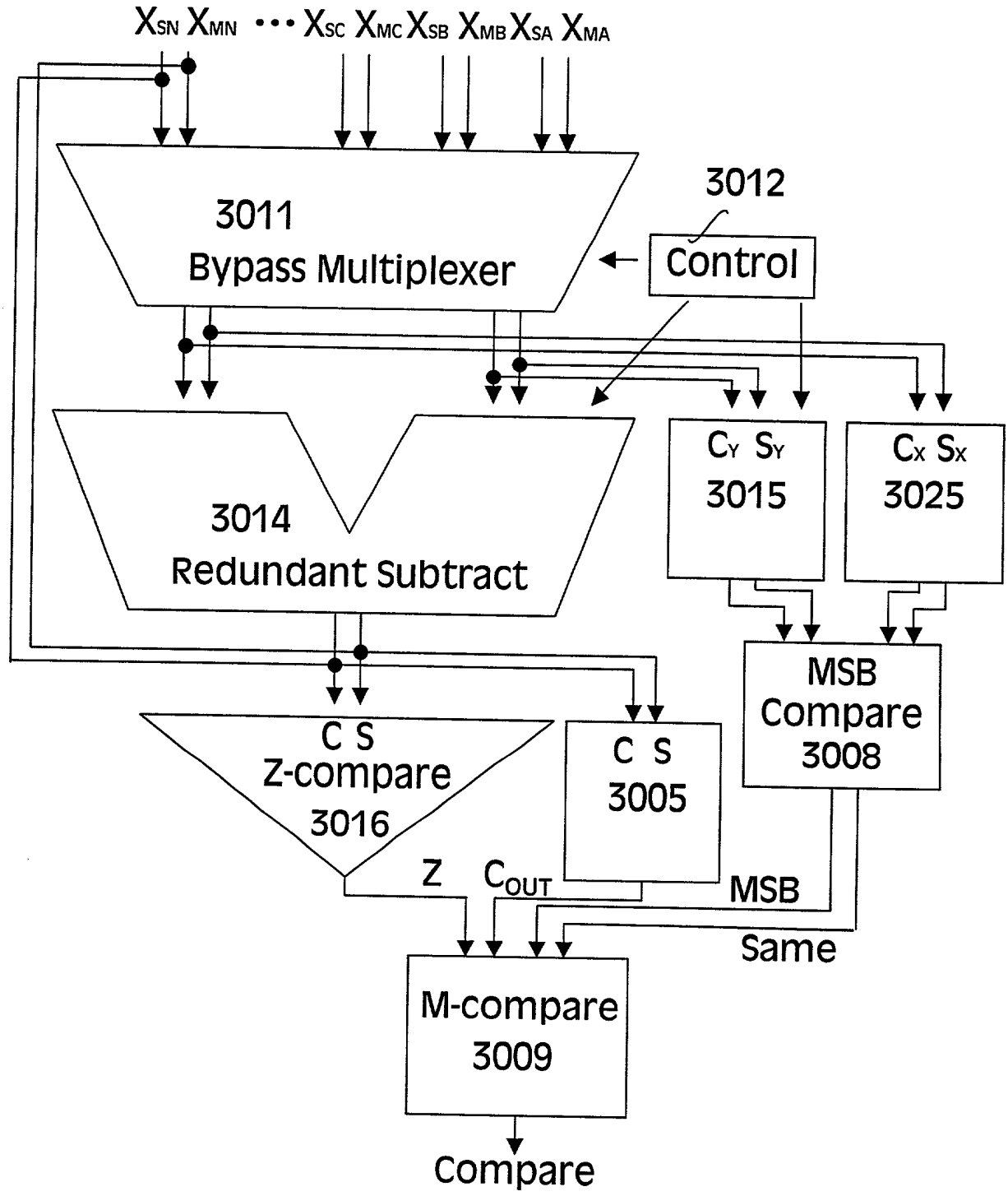
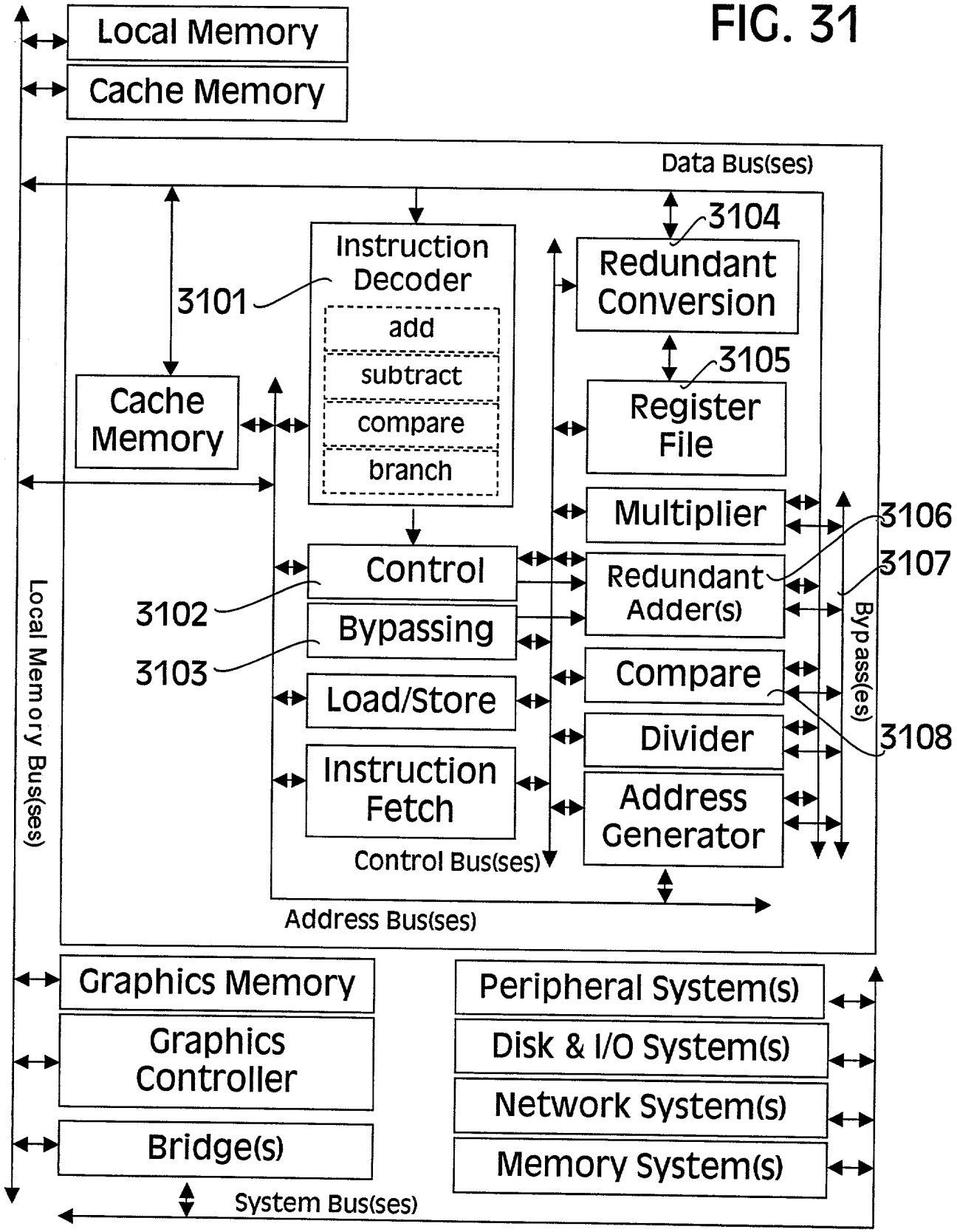

X_{SN} X_{MN} ••• X_{SC} X_{MC} X_{SB} X_{MB} X_{SA} X_{MA}
3011
Bypass Multiplexer
3012
Control
3014
Redundant Subtract
C_Y S_Y
3015
C_X S_X
3025
MSB
Compare
3008
C S
Z-compare
3016
C S
3005
Z
C_{OUT}
MSB
Same
M-compare
3009
Compare

FIG. 31


Local Memory
Cache Memory
Data Bus(ses)
3104
Instruction Decoder
3101
add
subtract
compare
branch
Redundant Conversion
3105
Register File
Cache Memory
Multiplier
3106
3107
Control
Redundant Adder(s)
3102
Bypassing
3103
Compare
Load/Store
Divider
3108
Instruction Fetch
Address Generator
Control Bus(ses)
Address Bus(ses)
Local Memory Bus(ses)
Bypass(es)
Graphics Memory
Peripheral System(s)
Graphics Controller
Disk & I/O System(s)
Network System(s)
Bridge(s)
Memory System(s)
System Bus(ses)